CIRCUITS AND SYSTEMS FOR ON-CHIP RF CHEMICAL SENSORS AND RF FDD DUPLEXERS

A Dissertation

by

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ABSTRACT

Integrating RF bio-chemical sensors and RF duplexers helps to reduce cost and area in the current applications. Furthermore, new applications can exist based on the large scale integration of these crucial blocks. This dissertation addresses the integration of RF bio-chemical sensors and RF duplexers by proposing these initiatives.

A low power integrated LC-oscillator-based broadband dielectric spectroscopy (BDS) system is presented. The real relative permittivity ε_r' is measured as a shift in the oscillator frequency using an on-chip frequency-to-digital converter (FDC). The imaginary relative permittivity ε_r'' increases the losses of the oscillator tank which mandates a higher dc biasing current to preserve the same oscillation amplitude. An amplitude-locked loop (ALL) is used to fix the amplitude and linearize the relation between the oscillator bias current and ε_r''. The proposed BDS system employs a sensing oscillator and a reference oscillator where correlated double sampling (CDS) is used to mitigate the impact of flicker noise, temperature variations and frequency drifts. A prototype is implemented in 0.18 μm CMOS process with total chip area of 6.24 mm^2 to operate in 1-6 GHz range using three dual bands LC oscillators. The achieved standard deviation in the air is 2.1 ppm for frequency reading and 110 ppm for current reading.

A tunable integrated electrical balanced duplexer (EBD) is presented as a compact alternative to multiple bulky SAW and BAW duplexers in 3G/4G cellular transceivers. A balancing network creates a replica of the transmitter signal for cancellation at the input of a single-ended low noise amplifier (LNA) to isolate the receive path from the transmitter. The proposed passive EBD is based on a cross-

connected transformer topology without the need of any extra balun at the antenna side. The duplexer achieves around 50 dB TX-RX isolation within 1.6-2.2 GHz range up to 22 dBm. The cascaded noise figure of the duplexer and LNA is 6.5 dB, and TX insertion loss (TXIL) of the duplexer is about 3.2 dB. The duplexer and LNA are implemented in 0.18 μm CMOS process and occupy an active area of 0.35 mm^2.

To my parents, my wife, my brother, and my kids

my heroes

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1. INTRODUCTION

Since the first integrated circuit, integration is a trend in the semiconductor industry to reduce the cost and minimize the size of products. Until now, there have been certain discrete radio frequency (RF) blocks that are difficult to integrate. There are two fields where there is room for more integration. The first application area is the biochemical sensors field. Biochemical sensors are used in industry, agriculture, medicine and environmental research. Biochemical sensors are conventionally bulky, expensive and require large amounts of samples for testing. An integrated biochemical sensor or a lab on a chip will be small in size, low-cost and requires minute amounts of a sample. In this thesis, a chemical sensor integrated prototype is designed that can measure real part of permittivity at 10 GHz. Another integrated prototype is designed, fabricated and tested to measure the complex permittivity of materials in the frequency range 1-6 GHz.

The second field is in mobile communication. Due to the fast progress in mobile communications, hand-held mobile handsets need to support multiple bands and standards. Software-defined-radio (SDR) is considered a solution to this dilemma with minimum cost and area. Tremendous progress has been achieved to solve issues related to SDR except for the required off-chip surface-acoustic-wave (SAW) RF duplexer. The SAW duplexer is needed to separate the RX signal from the TX signal in frequency division duplex (FDD) systems. Since there are numerous bands to support, an enormous area on the board is allocated to SAW duplexers and RF switches. A single integrated tunable RF duplexer can replace all these SAW duplexers and RF switches. Many challenges regarding integrating the RF duplexer are studied and analyzed in this dissertation. A CMOS prototype was designed, fabricated and

tested that addressed these problems.

1.1 Integrated Chemical Sensors

1.1.1 Chemical Sensing Applications

Objects and materials are defined by their characteristics. These characteristics are specified by the material properties: 1) electric properties, 2) magnetic properties, 3) thermal properties, etc. Electrical properties define the behavior of the material when it is applied to an electric field, while magnetic properties define the behavior of the material when it is applied to a magnetic field. Electrical properties are specified by conductivity (σ) and permittivity (ε). There are many applications where permittivity is used to determine the type of material (qualitative analysis) or its concentration in a solution (quantitative analysis).

Biomedical applications such as glucose meters, cell counter flow cytometers, and deoxyribonucleic acid (DNA) detection sensors are all based on electrical properties of the blood, cells, and DNA, respectively. Flow cytometers can also be used to distinguish between different cells. The variation of the output of the flow cytometer with frequencies can help to extract the electrical properties of the cells. Dead cells have a different response from living cells. Furthermore, cancerous cells can be differentiated from healthy cells. Even extraction of electrical properties of cancerous cells helps to identify the stage of cancer. The electric circuit should be very sensitive to distinguish these little variations from the noise.

1.1.2 Design Challenges of Integrated Dielectric Spectroscopy

Since the complex permittivity of materials changes with frequency, having the ability to measure complex permittivity with frequency helps to distinguish the material. Broadband dielectric spectroscopy (BDS) require high sensitivity and high dynamic range for a wideband frequency range. There are many challenges in de-

signing integrated biochemical sensor as a lab on a chip. There are electrical design problems: 1) high sensitivity to fine disturbance in the material under test (MUT), 2) minimizing the effect of ε' on reading ε'' and vice versa, 3) wideband frequency operation, 4) faster readout rates, 5) minimizing the consumption of materials used in testing. Also, there are big challenges with dealing with the chemical liquids on the surface of requiring stable microfluidic channels or on-chip chambers.

1.2 Integrated Frequency-Division Duplexing

During the evolution of the cellular communication, the method of separating the transmitted (TX) signal and the received (RX) signal has changed from generation to generation. Wireless mobile communication is a bi-direction communication using the same channel "full duplex". If the communication link is through single direction, it is called "half duplex". The single communication channel has many resources to be divided between TX and RX signals: time, frequency, spatial and polarization. Time division duplex (TDD) and frequency division duplex (FDD) are used in different generations of mobile communications. Spatial division duplex (SDD) can be used at millimeter frequencies since the antenna needs to have high directivity. In FDD, TX and RX signals are separated with a frequency separation called "full duplex" (FD) frequency, and higher order surface-acoustic-wave (SAW) filters are used to separate between TX and RX bands. The filters achieve out-of-band rejection greater than 50 dB. Since the first generation of mobile phone have analog communication system FDD was the suitable choice with frequency division multiple access (FDMA).

1.2.1 Motivation for Integrated FDD Duplexers

In the second generation (2G), Global System for Mobile Communications (GSM) introduces digital communication and time division multiple access (TDMA). TDD is used in 2G since it is similar to TDMA. Starting from the third generation (3G),

FDD was adopted to maximize the data rate by working all the time. The fourth generation (4G) has two versions: 4G-FDD used for high data rate communication and 4G-TDD. Since 4G mobile communication needs to support multiple bands using software-defined-radio (SDR), the design complexity of 4G-FDD increases since each band requires a separate off-chip SAW duplexer. The impacts on the area and the cost are enormous directing the research to solve this problem.

Since the frequency selectivity of SAW filters is defined by the mechanical cuts in their fabrication, they are impossible to tune. Finding a way to digitally tune an integrated high-performance RF duplexer will be of great importance to save cost and minimize the space required on board.

1.2.2 Design Challenges of Integrated FDD Duplexers

Since the filters require very high-quality factor ($Q > 100$) to implement low loss and high isolation duplexer, filtering technique can not be used to design the duplexer. All integrated duplexers used electrical balance concept to implement on-chip duplexers. Electrical balance duplexers (EBDs) are very similar to the hybrid transformer used in phone lines to convert the 4-wire link to 2-wire link. The method has its drawbacks: 1) there is higher insertion loss (IL) in the TX and RX signal paths with a physical limit on the summation of $TXIL$ and $RXIL$ is less than 6 dB, 2) antenna impedance is varying with time mandating a circuit to track this variation to preserve the high isolation between TX and RX, 3) the linearity of the duplexer should be very high since the intermodulation of the high power TX signal and any blocker received signal can affect the sensitivity of the receiver. These problems are very tough to solve, and the research in this area is still in its initial phase such that any progress in addressing any of the drawbacks is significant.

1.3 Objectives of the Dissertation

The central purpose of the dissertation is to integrate blocks that are conventionally needed to be off-chip. They are bulky and expensive, and their integration will reduce the total cost and the total size of the product. In order to achieve this aim, the thesis defines key objectives to reach.

The work on the biochemical sensor has four objectives:

- Sensitivity enhancement by reducing the effect of flicker noise, temperature and environment variations,
- Measuring complex permittivity ($\varepsilon = \varepsilon' - j\varepsilon''$),
- Maximizing the frequency range of operation such that it can be used as dielectric spectroscopy system,
- Minimizing the power consumption to assist in the portability of the device.

The work on the RF duplexer has three objectives:

- Studying the physical limits on $TXIL$ and $RXIL$ in passive EBDs (all passive components) and how to reduce them,
- Implement a prototype on chip EBD with low noise figure (NF) and low $TXIL$,
- Studying the benefits of using active EBDs (active + passive components) regarding NF and $TXIL$ and their effects on the linearity of the duplexer.

1.4 Dissertation Organization

The dissertation is divided into six main sections. In main section 2, the first section 2.1 has all the required definitions that are used in the chemical sensors. Section 2.2 shows the comparison among different types of techniques to measure

the permittivity. A proposed high accuracy LC-oscillator based chemical sensor is analyzed in section 2.3 where its measurements of measurements are shown in 2.3.5. In section 2.4, a flow cytometer module is presented using discrete components that can operate from 100 kHz to 50 MHz. Two types of breast cancer cells are differentiated from each other using the flow cytometer in sub-section 2.4.3. The section is concluded in sub-section 2.5.

In main section 3, a proposed wideband dielectric spectroscopy system is presented. Section 3.1 is the introduction for the sensor. Section 3.2 presents the theory of operation of the sensor. System simulations for the noise analysis are shown in section3.3 where the cancellation of flicker is verified by correlated double sampling (CDS). The implementations of the circuits are shown in section 3.4.Section 3.5.3 shows the measurements of the fabricated chip, while section 3.6 concludes main section 3.

The passive EBDs are analyzed main section4. Section 4.1 is the introduction for the EBD concept and current literature. Sections 4.2are 4.3 are comparing among different integrated EBD topologies. The circuit implementation and the measurements results of the prototype EBD are shown in 4.4 and 4.5, respectively. The performance of the prototype is concluded in section 4.6. Active EBDs are described in sections 5.1 and 5.2. Two implementations for integrated active EBDs are designed but not fabricated are shown in 5.3. The main section is summarized in 5.4.

Finally, section 6.1 concludes the work in the dissertation and the suggestions for future work are in 6.2.

2. DIELECTRIC SPECTROSCOPY SENSORS

Detection of chemicals and biological materials is vital in an enormous number of applications, including pharmaceutical, medical, oil, gas, and food/drug safety fields. A practical material detection approach involves characterizing physical and electrical properties of materials under test (MUTs), such as electrical permittivity [1]. The development of efficient permittivity detection techniques will benefit systems used for medical diagnosis and imaging, DNA sensing, material characterization, agricultural development, forensics, and bio-threat detection. Since many chemicals/biomaterials show significant changes at RF/microwave frequencies [1–7], permittivity detection in this band is particularly useful for chemical detection [5] and for medical applications, such as cell detection [4, 6] and blood-sugar monitoring [7].

2.1 Basic Definitions

2.1.1 Permittivity Definition

Assuming a parallel plate capacitor with area (A) spaced by distance (d), the voltage (V) applied on the capacitor will develop an electric field ($\overrightarrow{E}$) where $\overrightarrow{E} = \nabla V = E_0\vec{a}$ where E_0 is the scalar quantity of electric field and $\vec{a}$ is the unit vector to define direction. The charges stored in the capacitor (Q_0) in free space is proportional to the applied voltage by:

$$Q_0 = \frac{Q_0}{A}A = C_0\,V = C_0\,E_0\,d, \tag{2.1}$$

*© 2016 IEEE. Parts of section 2.3 are reprinted, with permission, from O. Elhadidy, M. Elkholy, A. A. Helmy, S. Palermo and K. Entesari, "A CMOS Fractional-N PLL-Based Microwave Chemical Sensor With 1.5% Permittivity Accuracy," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 9, pp. 3402-3416, Sept. 2013.

where C_0 is the ratio between the stored charge and applied voltage defined as the capacitance of the capacitor. If the capacitor is in free space, charge density (Q_0/A) is directly proportional to by:

$$\frac{Q_0}{A} = \varepsilon_0 E_0 \;\&\; C_0 = \varepsilon_0 \frac{A}{d}, \tag{2.2}$$

where ε_0 is the permittivity of free space ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m). If a homogeneous dielectric is introduced between the plates keeping the potential constant the charge stored is given by:

$$Q = A\,\varepsilon_0 \varepsilon_r\, E_0, \tag{2.3}$$

where ε_r is the dielectric constant of the material and ε ($\varepsilon = \varepsilon_0 \varepsilon_r$) is the permittivity of the material. The increase in the capability of storing charges for the same voltage or electric field is due the polarization of the material where [8]:

$$Q - Q_0 = A\,\varepsilon_0\, E_0\,(\varepsilon_r - 1)\,. \tag{2.4}$$

This increase may be attributed to the appearance of charges on the dielectric surfaces. Negative charges appear on the surface opposite to the positive plate and vice-versa (Fig. 2.1 found in [9]). This system of charges is apparently neutral and possesses a dipole moment (M_p):

$$M_p = A\,\varepsilon_0\, E_0\,(\varepsilon_r - 1)\,d. \tag{2.5}$$

Since the volume of the dielectric is $v = A\,d$, the dipole moment per unit volume is defined as polarization (P) of material:

$$P = \varepsilon_0 E_0 (\varepsilon_r - 1) = \chi \varepsilon_0 E_0, \tag{2.6}$$

where the constant is called the susceptibility $\chi = \varepsilon_r - 1$ of the material. The electric flux density D defined by:

$$D = \varepsilon_0 \varepsilon_r E_0 = P + \varepsilon_0 E_0. \tag{2.7}$$

Polarization of a dielectric may be classified according to:

1. Electronic or Optical Polarization
2. Orientational Polarization
3. Atomic or Ionic Polarization
4. Interfacial Polarization.

Each type of polarization has defined range of operation where the dipoles motion has a time constant (τ) and its behavior is changing with frequency {dispersion of the material}. Fig. 2.2 shows the different frequency ranges of the various types of polarizations [8]. Due to the relaxation of the polarization, the permittivity has real and imaginary components which are function of frequency ($\varepsilon_r = \varepsilon'_r - j\,\varepsilon''_r$).

2.1.2 Dielectric Frequency Dispersion and Mixture Theories

For pure MUTs, the complex permittivity frequency dependency follows the Cole–Cole model [10] and the complex permittivity numbers in [11]. The model is as follows:

$$\varepsilon_r = \varepsilon'_r - j\,\varepsilon''_r = \varepsilon_{r,\infty} \frac{\varepsilon_{r,0} - \varepsilon_{r,\infty}}{1 + (j\,\omega\,\tau)^{1-\lambda}}, \tag{2.8}$$

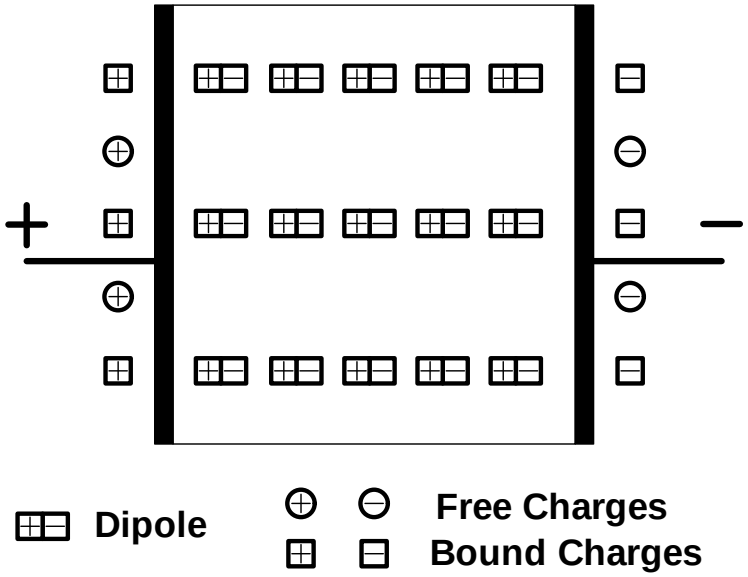


Figure 2.1: Schematic representation of dielectric polarization. [9]

where $\varepsilon_{r,0}$ is the static permittivity at zero frequency, $\varepsilon_{r,\infty}$ is the permittivity at ∞, τ is the characteristic relaxation time, and λ is the relaxation time distribution parameter. The dispersion of permittivity of distilled water (DI-water) at different temperatures is shown in Fig. 2.3 [12].

Binary mixtures are composed of two materials, which are: 1) the environment (host) and 2) the inclusion (guest) with ratios of $(1-q)$ and q, respectively. The complex permittivity of a binary mixture is a function of the complex permittivities of the two constituting materials and the fractional volume ratio . This relationship is mathematically defined as follows [13, 14]:

$$\frac{\varepsilon_{\text{eff}} - \varepsilon_e}{\varepsilon_{\text{eff}} + 2\,\varepsilon_e + \nu\,(\varepsilon_{\text{eff}} - \varepsilon_e)} = \frac{\varepsilon_i - \varepsilon_e}{\varepsilon_i + 2\,\varepsilon_e + \nu\,(\varepsilon_{\text{eff}} - \varepsilon_e)}, \tag{2.9}$$

where ε_{eff} is the effective mixture permittivity, ε_e is the permittivity of the environment, ε_i is the inclusion permittivity, and ν is a parameter to define the employed

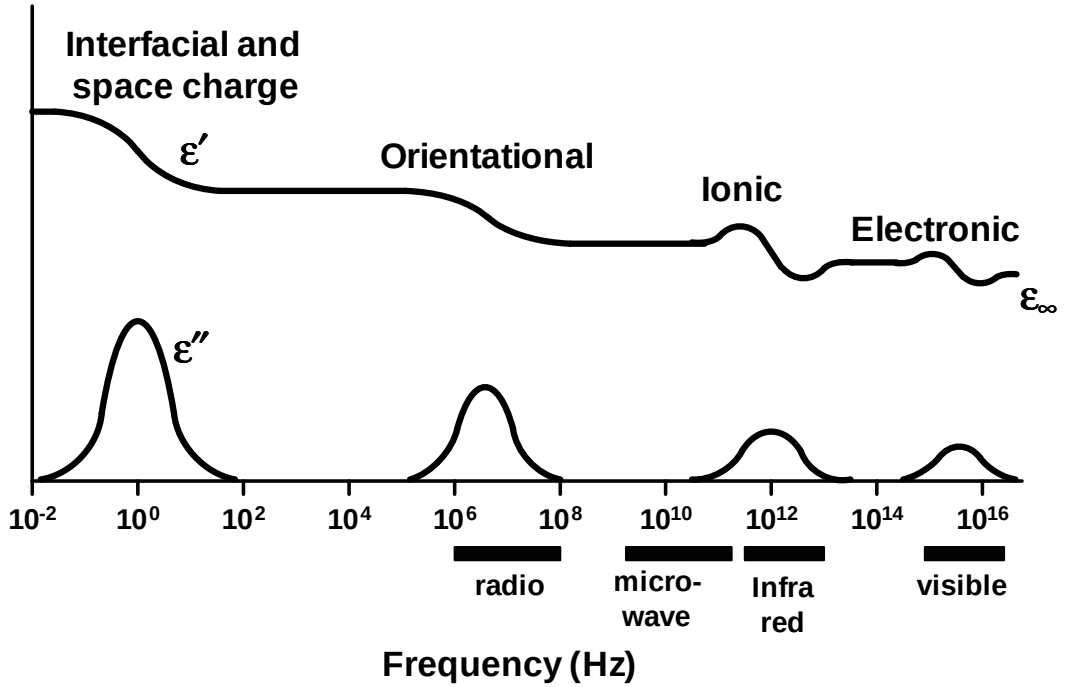
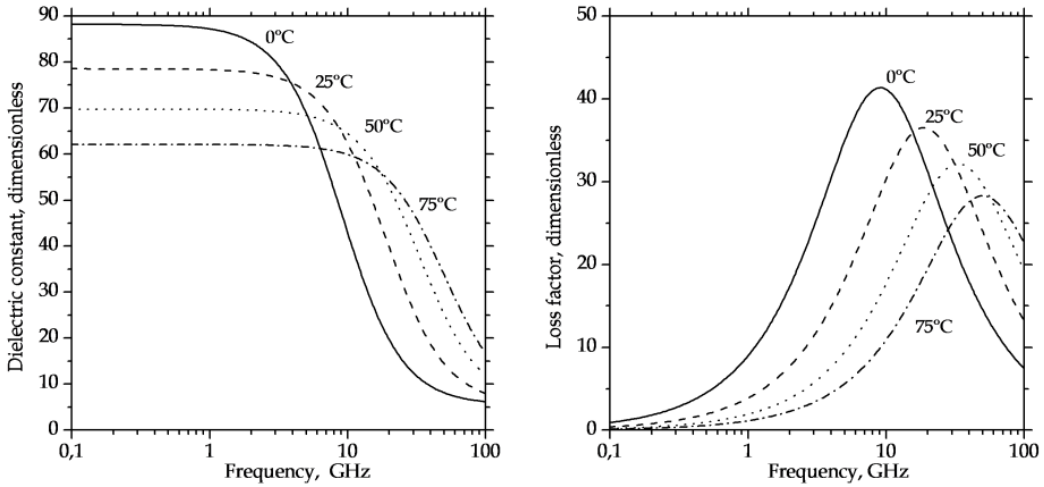


Figure 2.2: Frequency dependence of the real and imaginary parts of the dielectric constant (schematic). [8]

model. has values of 0, 2, and 3 corresponding to Maxwell–Garnett, Polder-van Santen, and quasi-crystalline approximation rules, respectively.

2.2 Dielectric Spectroscopy Background

There are different techniques to read the change in ε_r' and ε_r''. They can be divided into two categories: 1) Excitation-based measuring technique, 2) Oscillator-based measuring technique. In the excitation-based technique, there is an external source that defines frequency that is used in the measurement. For the oscillator-based technique, no external source is required since the measurement frequency is the oscillation frequency.



(a) (b)

Figure 2.3: The dispersion of distilled water at different temperatures: (a) dielectric constant ε_r' and (b) loss factor ε_r'' [12].

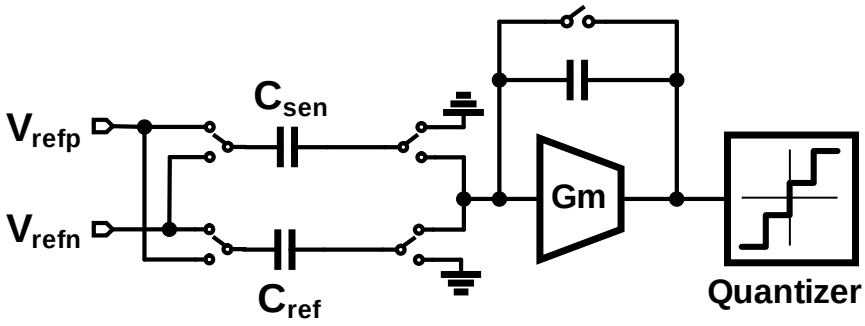


Figure 2.4: Implementation of the excitation based technique using switched capacitors circuit.

2.2.1 Excitation-Based Measuring Technique

There are different employments for the excitation-based measuring technique. The simplest one is using a switched capacitor circuit as a capacitive sensor. A reference voltage is applied on the sensor and reference capacitors and the difference

in charges is calculated, as shown in Fig. 2.4 [15]. Switched capacitors circuit techniques can be used to digitize the output using simple switched capacitor analog to digital converter (ADC). The advantages of this technique are simplicity and low power operation. It also has its drawbacks: 1) it can not be used to measure ε_r'', 2) it suffers from harmonics problems which minimize its use in measuring ε_r' versus frequency, 3) it has higher noise level due to aliasing of the noise of the operational transconductance amplifier (OTA), 4) it can be used at low frequencies only.

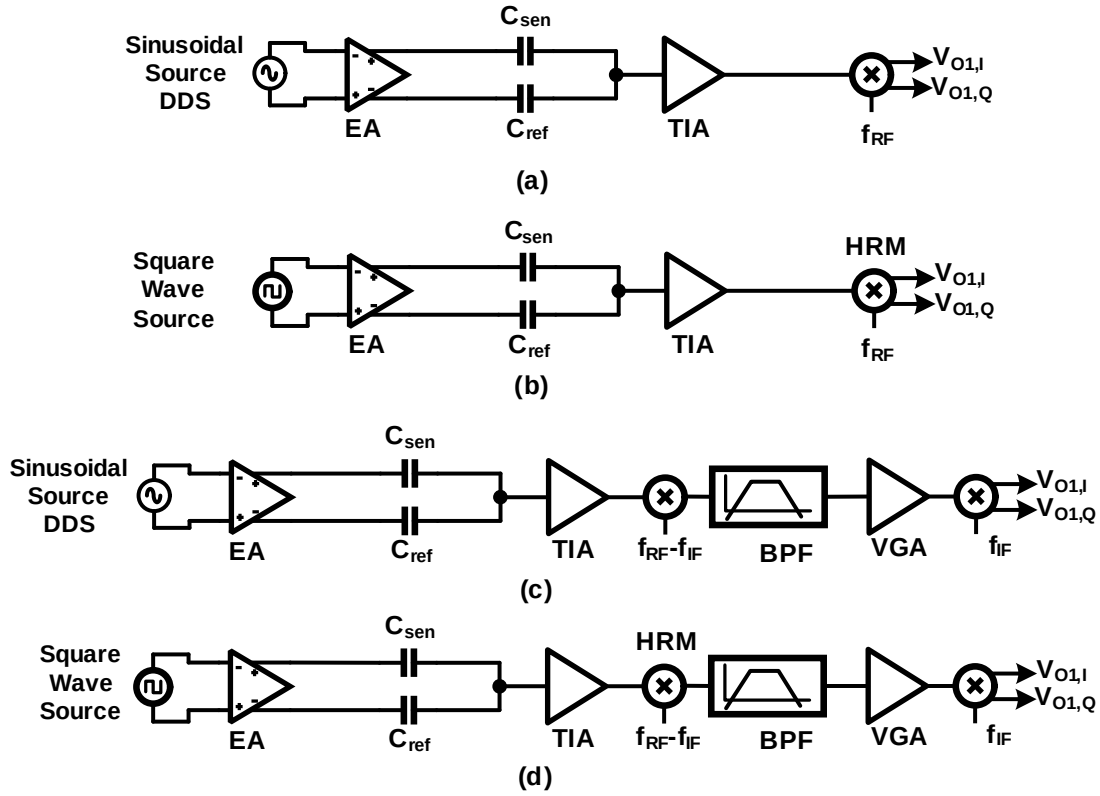


Figure 2.5: Different implementations of the excitation based technique using TIA: (a) a sinusoidal excitation signal and a single stage mixer, (b) a square-wave excitation signal and a single stage harmonic rejection mixer, (c) a sinusoidal excitation signal and a two stage mixer and (d) a square-wave excitation signal and a two stage harmonic rejection mixer.

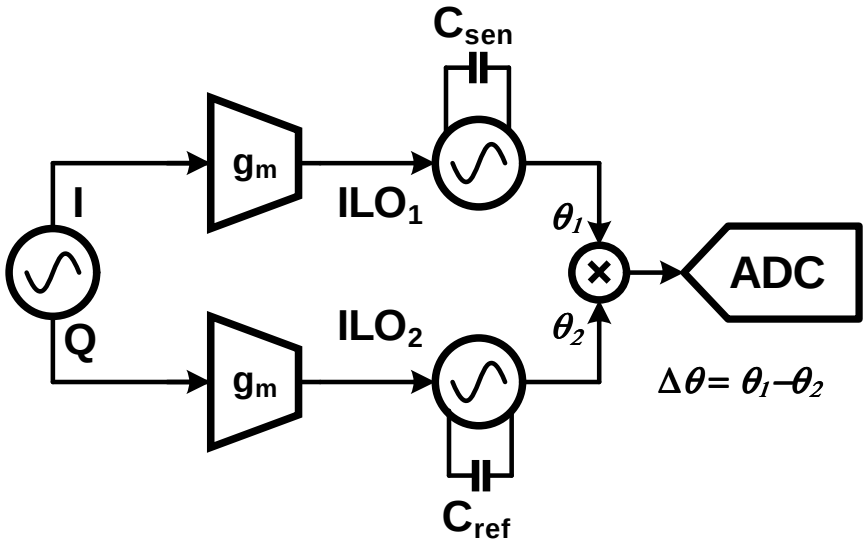


Figure 2.6: Reading the change in capacitance as a change in the phase of ILOs.

Another technique is shown in Fig. 2.5(a). A differential excitation signal is applied on the sensing and reference capacitors. The currents that are passing through these capacitors is added and converted to a voltage using a trans-impedance amplifier (TIA). The TIA should have very low input resistance to minimize its effect on the measurements. Furthermore, the TIA should have very low input referred noise since its noise dominates the noise of the system. It can measure ε_r' and ε_r''using quadrature mixers after the TIA and can operate continuously from low frequencies till moderate frequencies. This technique has its drawbacks: 1) it needs sinusoidal excitation source which is not easy to generate, 2) the dc offset and flicker noise of the mixers can affect the noise of the system, 3) high power consumption, 4) it needs external source with wide frequency range. The sinusoidal source can be replaced by a square-wave signal, but the harmonics of the square-wave signal will generate output due to higher order harmonics. To minimize the effects of the harmonics differential mixers are used to eliminate even order harmonics and 8-phases (16-phases)

harmonic rejection mixers are used to cancel the 3^{rd} and the 5^{th} harmonics (up to the 13^{th}harmonic), as shown in Fig. 2.5(b) [16]. The dc-offset and flicker noise of the mixers can be solved using low IF superheterodyne receiver with an IF frequency near 1 MHz [17], as shown in Fig. 2.5(c) and (d).

Another excitation-based technique is using an injection-locked oscillator (ILO) to be locked at a particular frequency using an external source, as shown in Fig. 2.6 [18]. This technique is similar to the oscillator-base technique, but the change in capacitance changes the relative phase of oscillation. A phase detector (PD) measures the phase difference between the sensor and reference ILOs phases. This technique can achieve very high sensitivity in measuring ε_r' even at very high frequencies. It has drawbacks too: 1) its dynamic range is tiny since the ILO is out of lock for significant frequency shifts, 2) measuring ε_r'' is hard since the injection complicates the relation between ε_r'' and the oscillation amplitude.

2.2.2 Oscillator-Based Measuring Technique

Table 2.1: Comparison Among Different Techniques to Measure Permittivity

	Excitation Based Tech.			Oscillator Based Tech.	
	Switched Cap.	Using TIA	Injection Locked Osc.	Ring Osc.	LC Osc.
Operating Freq.	low	low to high	high	moderate to high	high
Freq. Range	wide	wide	very narrow	wide	moderate
Freq. Programmability	easy	easy	difficult	easy	difficult
External Source	yes	yes	yes	no	no
Reading ε_r''	no	yes	no	yes	yes
Sensitivity in ε_r'	moderate	moderate	high	moderate	high
Sensitivity in ε_r''	NA	moderate	NA	moderate	moderate
Dynamic Range in ε_r'	moderate	moderate	medium	moderate	high
Dynamic Range in ε_r''	NA	moderate	NA	low	low
Harmonics Problem	yes	yes	no	no	no

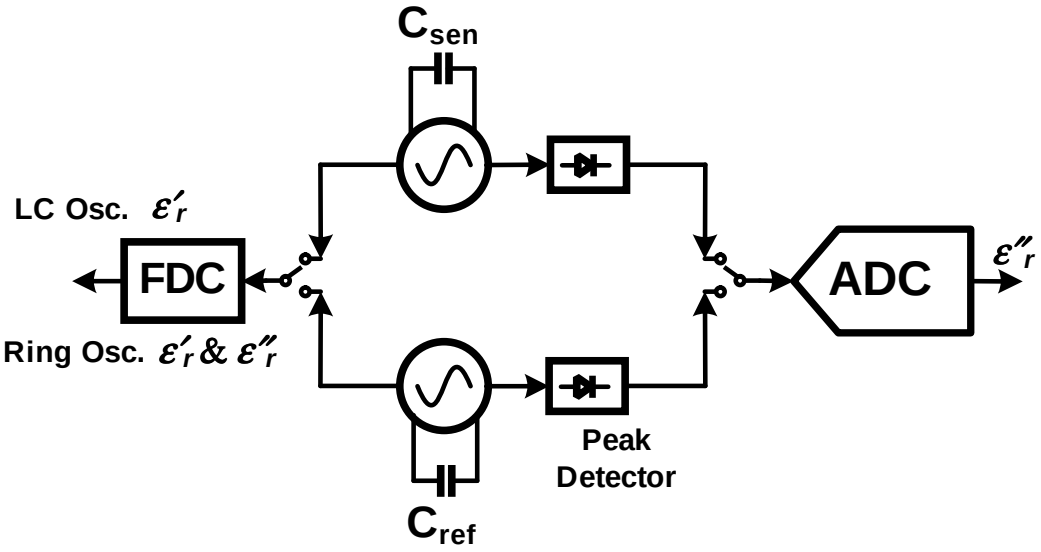


Figure 2.7: Reading ε_r' and ε_r'' using the frequency and amplitude of the oscillator.

Oscillator based measuring technique is simpler than the excitation-based technique. The sensing and reference capacitors are used in sensing and reference oscillators, respectively. Each oscillator has two outputs: frequency and amplitude, as shown in Fig. 2.7. In LC-oscillators, the frequency is determined by inductance L and capacitance C. Therefore, ε_r' can be found directly using the frequency with high sensitivity with low dc power consumption [1, 19]. Frequency is converted into digital using frequency-to-digital converter (FDC) which can be as simple as a counter. However, in ring oscillators, the frequency is determined by the capacitance C and the loss. Measuring complex permittivity using ring oscillators can be achieved with moderate sensitivity in reading ε_r' and ε_r'' [20]. Although ring oscillators can operate at very wide frequency range, dc power consumption at high frequencies is much higher compared to LC oscillators. Furthermore, ring oscillators are noisier and their frequency is not stable compared to LC oscillators.

In the oscillator-based technique, there is no need for an external source, but the

frequency is not controlled. To define the frequency of measurement, an integer-N phase-locked loop (PLL) is used to control the frequency [1,20]. Table 2.1 summarizes the comparison among the different techniques.

2.3 High Accuracy Chemical Sensor Prototype

Capacitance-based sensing, where a capacitor exposed to an MUT exhibits changes in electrical properties, is a conventional technique reported in the literature for permittivity detection. Low-frequency charge-based methods to detect capacitance changes include embedding biomaterial sensitive capacitors in a relaxation oscillator [21] and as load devices for charge integration with precisely controlled current sources [15]. Another example in the 10-MHz range is an impedance spectroscopy approach [22], where a sinusoidal voltage source excites a material-sensitive capacitor and the impedance magnitude and phase is extracted with a coherent detector.

However, the techniques mentioned above are not well suited for permittivity detection at microwave frequencies. For microwave permittivity sensing, one approach is to detect the sensor's reflection and or transmission properties to characterize the MUT [7,23,24]. A drawback of these approaches is that they require somewhat large transducer structures, especially if scaled to the 10-GHz range. Another microwave-based technique is to deposit the MUT on top of a microwave resonator and observe the permittivity change as a shift in the resonance frequency. While onboard sensors have been implemented using this resonant-based technique, [23], fully integrated permittivity sensors at microwave frequencies are necessary for compact size and low cost to be suitable for lab-on-chip and point-of-care applications.

In [1], a CMOS integrated microwave chemical sensor based on capacitive sensing is proposed with an LC voltage-controlled oscillator (VCO) that utilizes a sensing capacitor as a part of its tank. The real part of the permittivity of the MUT applied

on the sensing capacitor changes the tank resonance frequency, and hence, the VCO free-running frequency. Embedding the material sensitive VCO in a phase-locked loop (PLL) allows the oscillator free-running frequency shift to be translated into a change in the control voltage, which is read by an analog-to-digital converter (ADC). A multi-step detection procedure, with the ADC output bits controlling an external tunable reference oscillator to equalize the control voltage in both the presence and absence of the material, is then used to read-out the sensor oscillator frequency shift. While this system was able to measure the real part of the permittivity of organic chemicals and binary organic mixtures in the range of 7–9 GHz with a 3.5% error, defined as the absolute difference between the room temperature (20° C) measured and theoretical values [10, 11], it suffers from several drawbacks, which are: 1) an expensive tunable reference frequency source is required; 2) the ADC resolution limits the accuracy of the frequency shift detection, and 3) utilizing a single VCO sensor necessitates a complicated multi-step measurement procedure and makes the system performance susceptible to low-frequency environmental variations.

This paper presents a CMOS fractional-N PLL-based chemical sensor based on detecting the real part of an MUT's permittivity. Detection of this real part of the permittivity is suitable for the characterization of mixing ratios in mixtures, which is beneficial in many applications, including 1) medical applications such as the estimation of the glucose concentration in blood [7] and 2) the estimation of moisture content in grains [25]. The system utilizes both a sensor and reference VCO, which enables improved performance and lower complexity compared to the system in [1]. For the frequency-shift readout, instead of controlling an expensive externally tunable reference oscillator, a low-complexity bang–bang control loop periodically compares the control voltage when the sensor and the reference oscillator are placed in the PLL loop and adjusts a fractional- loop divider. Since the system determines

permittivity by measuring the frequency difference between the sensor and reference VCO, common environmental variations are canceled out, and the measurement procedure is dramatically simplified to a single-step material application. Also, utilizing a high-resolution fractional divider allows the frequency shift resolution measurement to be limited by system noise, rather than the ADC quantization noise [1]. This section is organized as follows. Sub-section 2.3.1 discusses VCO-based sensing systems and provides an overview of the proposed fractional- PLL-based chemical sensor system. Key design techniques for the capacitive sensor and the VCO, which is optimized to minimize the effect of the imaginary part of the permittivity on the oscillation frequency to ensure the real part is accurately detected, are discussed in Sub-section 2.3.2. Sub-section 2.3.3 provides more circuit implementation details of the shared bias sensor and reference VCO, other PLL blocks, and the bang–bang comparator, which senses the VCO control voltage. The 90-nm CMOS prototype and the chemical sensing test setup are detailed in Sub-section 2.3.4. Sub-section 2.3.5 shows the experimental results, including characterization of the major circuit blocks and organic chemical mixture detection measurements.

2.3.1 VCO-Based Sensing Systems

This section first details leading features of VCO-based sensing systems. The proposed fractional- PLL-based sensor system is then described.

2.3.1.1 VCO-Based Sensor Characteristics

A VCO-based sensor is composed of a sensing VCO and a frequency detector to detect a frequency shift, Δf, as shown in Fig. 2.8(a). The frequency resolution, defined as the minimum frequency shift that can be detected by the system, is primarily a function of the system's input referred noise and frequency detector quantization noise. Note that both the VCO phase noise and the frequency detector

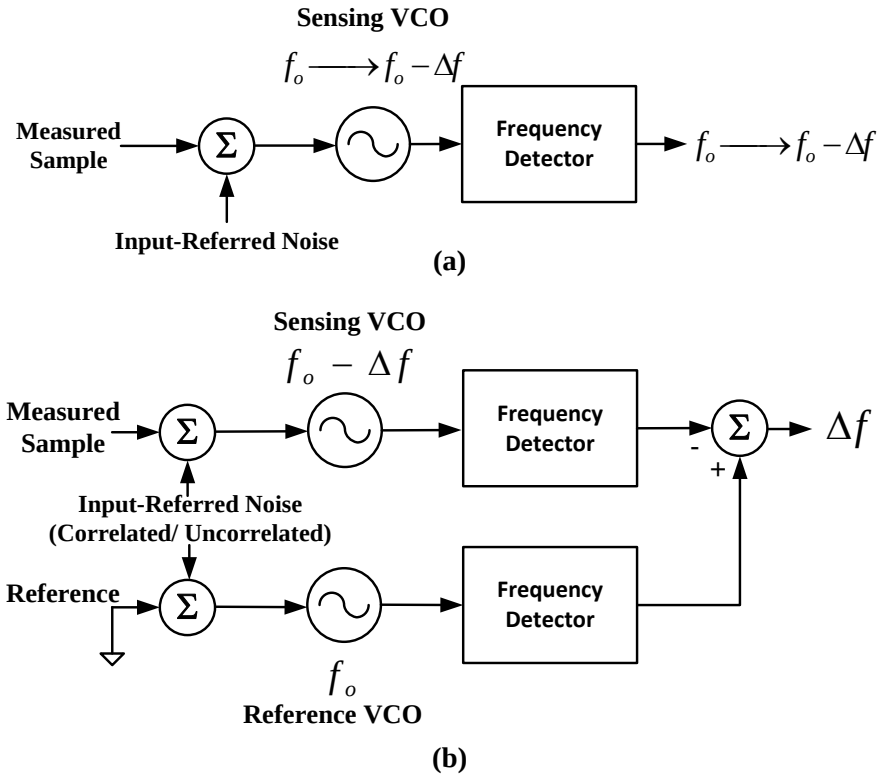


Figure 2.8: VCO-based sensors incorporating: (a) a single VCO and (b) reference and sensing VCOs.

circuitry can contribute to the system's input-referred noise. The performance of the sensing system in Fig. 2.8(a) is limited by VCO temperature sensitivity and low-frequency noise. This behavior motivates the use of a reference oscillator [19], as shown in Fig. 2.8(b), and measuring the desired frequency shift as the difference between the sensing and the reference VCOs. One practical issue with this approach is that the two VCOs should be in close proximity to maximize noise correlation. However, this causes VCO frequency pulling when the VCOs are simultaneously operating. In order to avoid this, the two VCOs can be periodically activated such that only one operates at a time [19]. This chopping results in a beneficial high-pass filtering of the correlated low-frequency noise between the sensor and reference VCO.

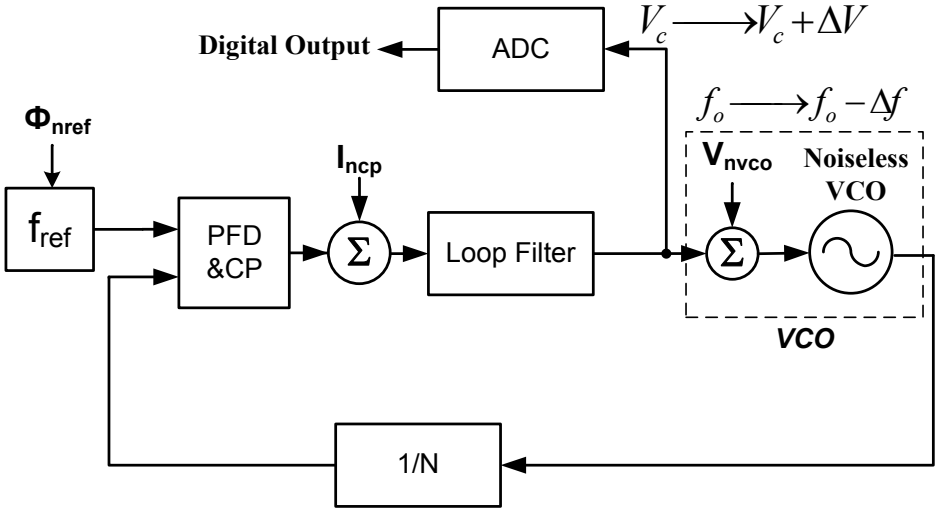


Figure 2.9: VCO-based sensor using a PLL and an ADC as a frequency detector [1].

One common frequency detector implementation is a frequency counter [19]. While this method can achieve high resolution, it requires long measurement times, on the order of milliseconds. Also, since the VCOs are embedded in an open loop system, the absolute oscillator frequency drift makes it difficult to characterize the MUT properties at a precise frequency.

A PLL can serve as a closed-loop frequency detector circuit, as shown in Fig. 2.9 [1], to enable MUT characterization at a precise frequency. For a fixed division ratio, N, and reference frequency, f_{ref}, the change in the VCO free-running frequency is translated into a change in the control voltage, V_c, and read out using an ADC. This method also offers a significantly faster measurement time set by PLL settling, typically on the order of microseconds, which is useful for high-throughput chemical characterization systems and emerging biosensor platforms for real-time monitoring of fast biological processes, such as protein- drug binding kinetics [26].

In addition to the VCO, the other blocks in the PLL-based system also contribute to system noise and should be analyzed by considering the transfer function from

that particular block to the control voltage node. The PLL filters high-frequency content of the VCO input-referred noise, $V_{n,vco}$, as the transfer function, $V_{n,vco}/V_c$, is a low-pass response with a cutoff frequency equal to the loop bandwidth [1], while noises from the charge pump (CP), $I_{n,cp}$, and input reference clock, $\phi_{n,ref}$, are band-pass filtered by the loop. Also, in the locked condition, the CP noise is scaled due to it only appearing on the control voltage for a time equal to the reset path delay of the phase-frequency detector (PFD) [27], which is a fraction of a reference clock cycle. Assuming a low-noise input reference clock, the VCO noise and CP noise are dominant. However, care should also be used in choosing the loop filter resistor, as its noise on the control voltage is high-pass filtered by the loop. Note, an important trade-off exists between the control voltage noise level and the PLL settling time, as reducing the PLL bandwidth filters more VCO input-referred noise and CP noise at the cost of increasing the system measurement time. Another important noise source, the system quantization noise, is set by the ADC resolution [1]. This implies a significant increase in ADC resolution requirements and overall complexity for improved frequency shift measurement capabilities.

2.3.1.2 VCO-Based Sensor Characteristics

As mentioned before, the use of a reference VCO enables filtering of correlated low-frequency noise between the sensor and reference VCOs. This correlation is achieved in a PLL-based system with the proposed sensor architecture shown in Fig. 2.10. Here, the PLL utilizes a single fixed reference clock and is controlled by f_S the clock, which alternates between having the sensor oscillator and fixed integer divider, N_S, in the loop and having the reference oscillator and adjustable fractional divider, N_R, present.

When f_S is in the low state, the reference VCO frequency, $f_{vco,R}$, is set to $8 \times$

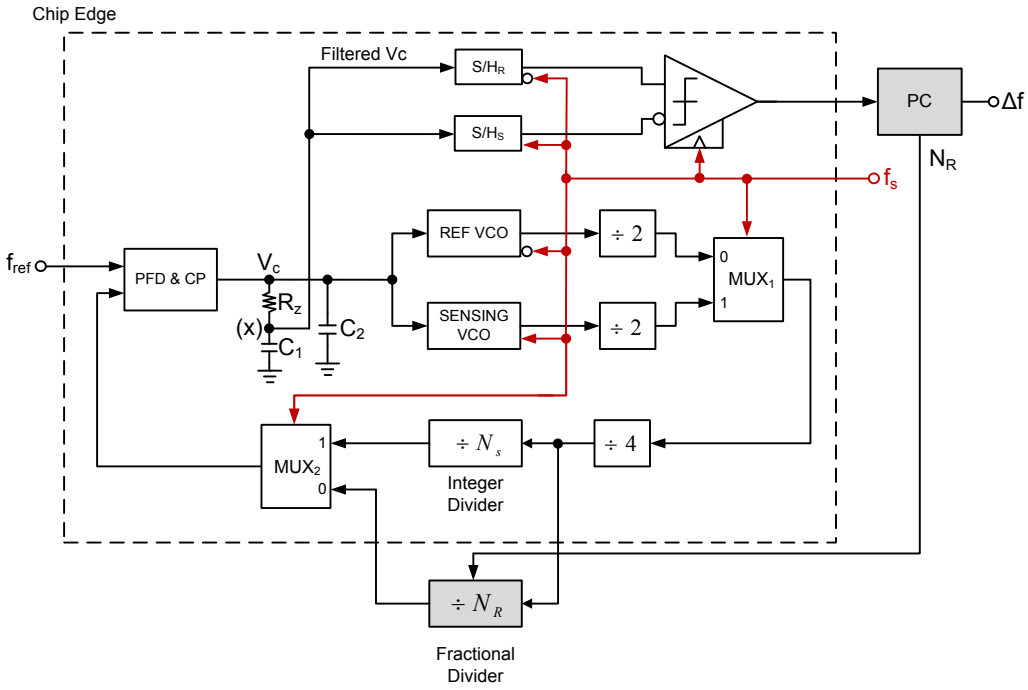


Figure 2.10: Block diagram of the dielectric sensor based on a fractional-N frequency synthesizer with sensor and reference VCOs and dual-path loop dividers. A bang–bang control loop adjusts the fractional divider value to determine the frequency shift between the sensor and the reference VCO.

$N_R \times f_{ref}$ and the control voltage settles to $V_{c,R}$, while when f_S is in the high state, the sensor VCO frequency, $f_{vco,S}$, is set to $8 \times N_R \times f_{ref}$ and the control voltage settles to $V_{c,S}$. Assuming that the two division values are equal, $N_R = N_S$, the difference between $V_{c,R}$ and $V_{c,S}$ is a function of the MUT induced frequency shift between the two VCOs and

$$f_{vco,R} = f_o + K_{vco} V_{c,R}, \tag{2.10}$$

$$f_{vco,S} = f_o - \Delta f + K_{vco} V_{c,S}, \tag{2.11}$$

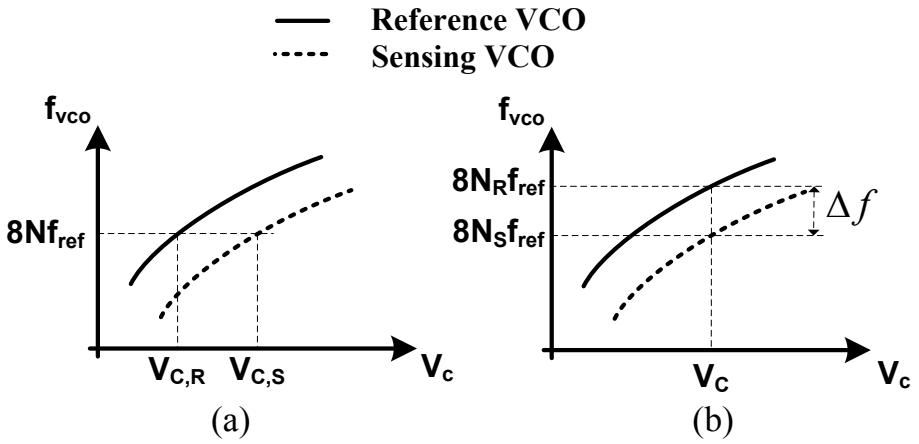


Figure 2.11: VCO frequency versus control voltage. (a) $N_R = N_S = N$, (b) $V_{c,R} = V_{c,S} = V_c$.

where K_{vco} is the VCO gain in Hz/V, f_o is the free-running frequency of the reference VCO, and Δf is the difference between the free-running frequencies of the reference and sensing VCOs, which is the subject of detection. Substituting $f_{vco,R} = 8\,N_R\,f_{ref}$ and $f_{vco,S} = 8\,N_S\,f_{ref}$ results in

$$8\,N_R\,f_{ref} = f_o + K_{vco}V_{c,R}, \tag{2.12}$$

$$8\,N_S\,f_{ref} = f_o - \Delta f + K_{vco}V_{c,S}. \tag{2.13}$$

Thus, as shown in Fig. 2.11(a), the frequency shift can be approximated as

$$\Delta f = K_{vco}\,(V_{c,S} - V_{c,R})\,. \tag{2.14}$$

However, measuring the frequency shift based on the difference between $V_{c,R}$ and $V_{c,S}$ suffers from two drawbacks, which are: 1) the accuracy is degraded due to the VCO gain non-linearity and 2) a high-resolution ADC is required. Using (2.14), the

relationship between the VCO frequency, frequency shift in ppm, the average VCO gain K_{vco}, supply voltage, V_{DD}, and the number of ADC bits, N_{ADC}, is

$$\Delta f \text{ (ppm)} = \frac{V_{DD}\, 10^6}{2^{N_{ADC}}} \times \frac{K_{vco}}{f_{vco}}. \tag{2.15}$$

For example, if $V_{DD} = 1.2$ V,$K_{vco} = 500$ MHz/V, and $f_{vco,S} = 10$ GHz, an ADC with a minimum 10-bit resolution is required to detect frequency shifts in the order of ∼60 ppm. The following describes how these two drawbacks are mitigated by a different detection algorithm and a bang–bang control loop.

In order to eliminate the effect of VCO gain non-linearity, a different detection algorithm is used that is based on changing the division value, N_R, until the control voltage $V_{c,R}$ becomes equal to the control voltage $V_{c,S}$, as shown in Fig. 2.11(b).Here, the difference between N_R and N_S represents the frequency shift between the two VCOs,

$$\Delta f = 8\, f_{ref}\, (N_S - N_R)\,. \tag{2.16}$$

Here, the frequency shift measurement is independent of the VCO gain non-linearity. However, the measurement accuracy is still limited by the reference frequency value and the resolution of the adjustable frequency fractional divider. As reducing the reference frequency mandates reducing the PLL bandwidth, which increases the PLL settling time, this system employs an off-chip fractional divider, N_R. While this fractional divider could easily be implemented in the CMOS chip, since designing high-resolution dividers is much easier than high-resolution ADCs, due to tape-out time constraints an external divider was used in this prototype, as shown in Fig. 2.10. A fractional divider with M-bit fractional resolution provides a minimum frequency shift of $\Delta f_{min} = \left(f_{ref}/2^M\right)(10^6/f_{vco})$. For example, utilizing a 25-MHz

reference frequency, 10-GHz VCO frequency, and a 25-bit fractional divider results in a resolution of 7.7×10^{-5} ppm.

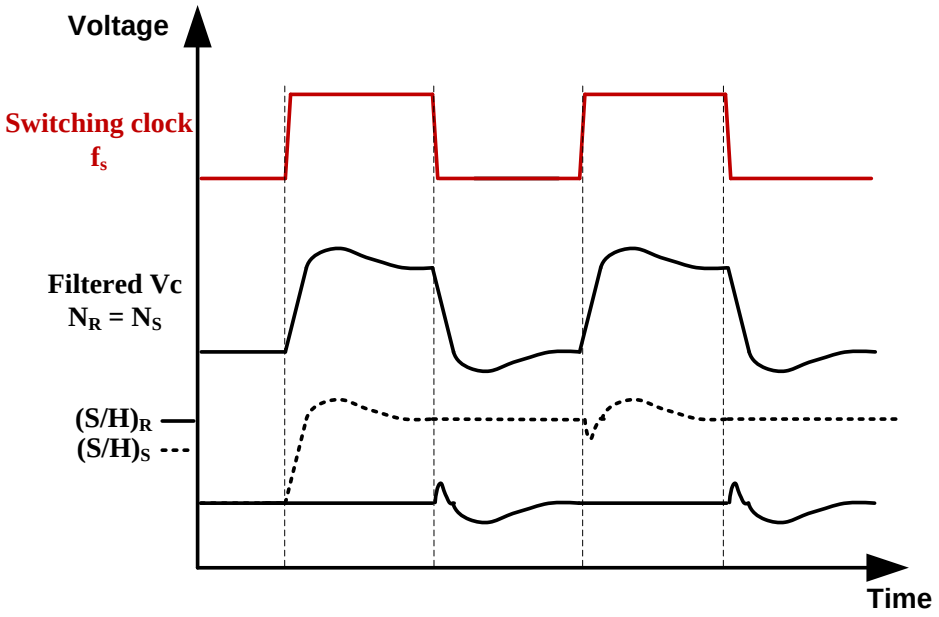


Figure 2.12: System signals: sensor/reference control f_S, filtered control voltage V_c, and output of sample and hold circuits.

In order to alleviate the need for a high-resolution ADC, a bang–bang control loop is used to adjust the divider value. Here the term "bang–bang" indicates that the control loop's error detector, which is a comparator, generates only a quantized logical " -1" or " +1" depending only on the error sign, similar to the operation of a bang–bang phase detector used in clock-and-data recovery (CDR) systems [28]. As illustrated in Fig. 2.12, the control voltage is sampled during each phase of the switching clock, f_S, using sample and hold circuits $(S/H)_R$ and $(S/H)_S$ and applied to a comparator. The comparator output is used to adjust the fractional divider value and determine the frequency shift. A cumulative density function (CDF) of

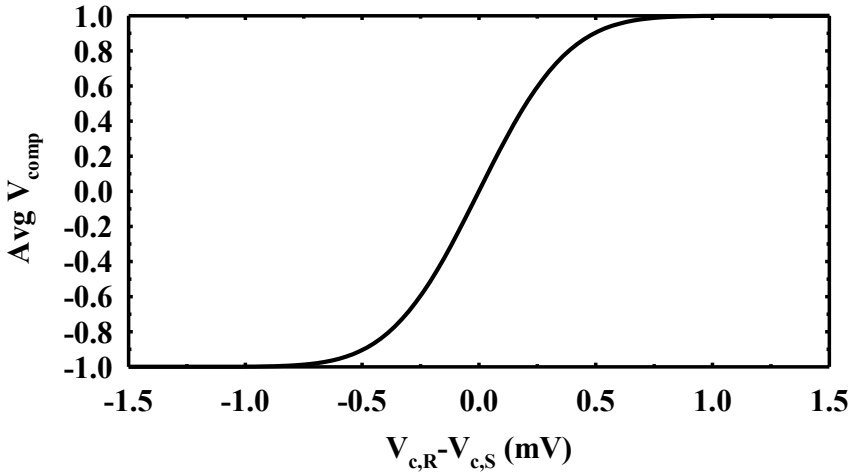


Figure 2.13: CDF function that represents the averaged comparator output versus the difference between $V_{c,R}$ and $V_{c,S}$ with $\sigma_{Vc} = 25$ mV, which corresponds to 15 ppm at $K_{vco} = 500$ MHz/V.

the average comparator output, V_{comp}, versus the difference between $V_{c,R}$ and $V_{c,S}$ is shown in Fig. 2.13, assuming Gaussian system noise. If the average comparator output is near a logical " -1" or " +1," the difference between $V_{c,R}$ and $V_{c,S}$ is significantly larger than the total system noise and the system uses the averaged comparator output to adjust the reference divider. As the difference between $V_{c,R}$ and $V_{c,S}$ moves toward zero, the system noise causes the comparator to output a similar number of " -1" and " +1" outputs, and the averaged output approaches zero. Once the averaged comparator output is near zero to within a certain tolerance, the frequency shift is then calculated. As the sensor divider remains fixed, this approach ensures that the frequency shift is measured at a fixed frequency, regardless of the frequency shift.

The flowchart of Fig. 2.14 summarizes the system operation as follows:

1. The MUT is deposited on top of the sensing VCO.

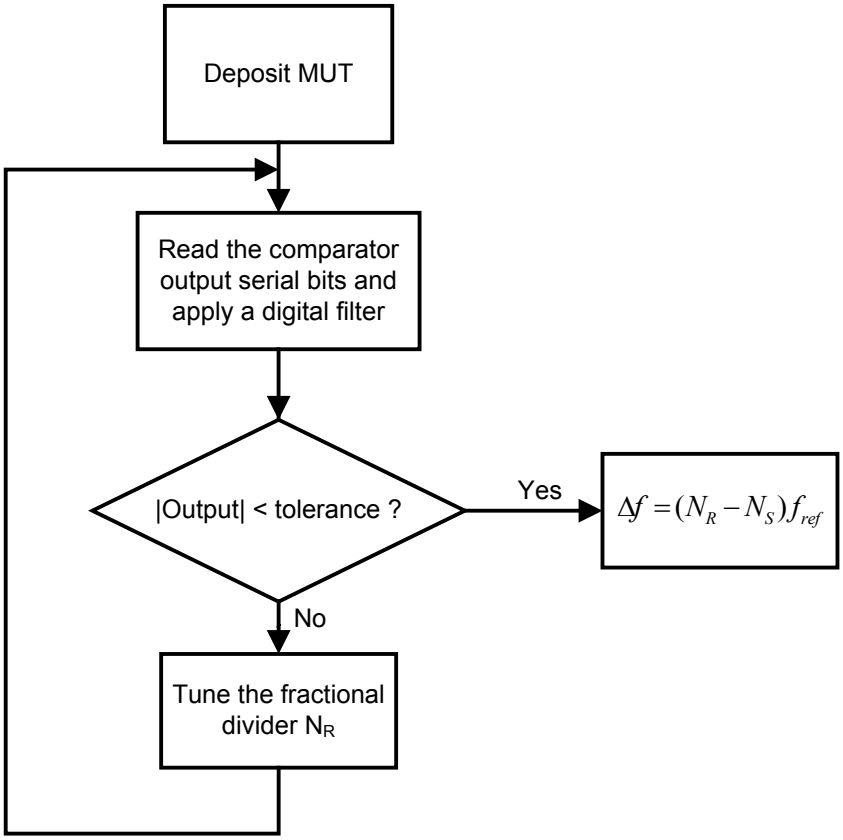


Figure 2.14: Flowchart of the frequency shift measurement algorithm.

2. The comparator output bits are read out to a PC and digitally filtered.

3. The division ratio, N_R, is tuned until the average comparator output approaches zero.

4. At which, the frequency shift is measured as f_{ref} $(N_R - N_S)$.

Note that this measurement procedure requires only a single MUT application, and is dramatically simpler than the multi-step MUT application and de-application procedure of [1]. Several techniques are utilized to improve the system noise performance and account for mismatches between the sensor and reference VCO. A filtered version

of the PLL control voltage at node X (Fig. 2.10) is sampled to filter high-frequency noise. Additional low-frequency noise filtering is also possible by increasing the averaging time of the comparator outputs. As the mismatches between the two VCOs and the comparator input-referred offset introduces a systematic system offset, this is accounted for during sensor calibration by characterizing the system with the sensing VCO not loaded with any MUT. For this calibration case with the sensor only exposed to air, the difference between N_R and N_S is read out, recorded, and serves as the overall system offset. Note that this offset calibration should be performed at each material characterization frequency in order to account for the VCOs' K_{vco} variation with frequency. In addition, any K_{vco} mismatch between the VCOs can be calibrated by performing measurements with control materials of known permittivity; with system accuracy improving with the number of calibration materials employed. Additional sensor calibration details are provided in the experimental results of sub section 2.3.5.2.

2.3.2 Sensor Design

2.3.2.1 Sensing Element

Each MUT has a frequency-dependent complex relative permittivity $\varepsilon_r(\omega) \triangleq \varepsilon_r'(\omega) - j\varepsilon_r''(\omega)$ with both real and imaginary components. The real part represents the stored energy within the material and the imaginary part represents the material's loss with the loss tangent quantifying the ratio between $\varepsilon_r''(\omega)$ and $\varepsilon_r'(\omega)$ ($\tan\delta = \varepsilon_r''(\omega)/\varepsilon_r'(\omega)$). As the objective of the implemented sensor is to detect the real part of the MUT's complex permittivity, the MUT is placed on top of a capacitor-based sensor, and the permittivity is measured with the change in the sensor's capacitance. This section explains the sensor's design and essential characteristics. It also discusses the effect of the material's loss on the capacitance measurements and

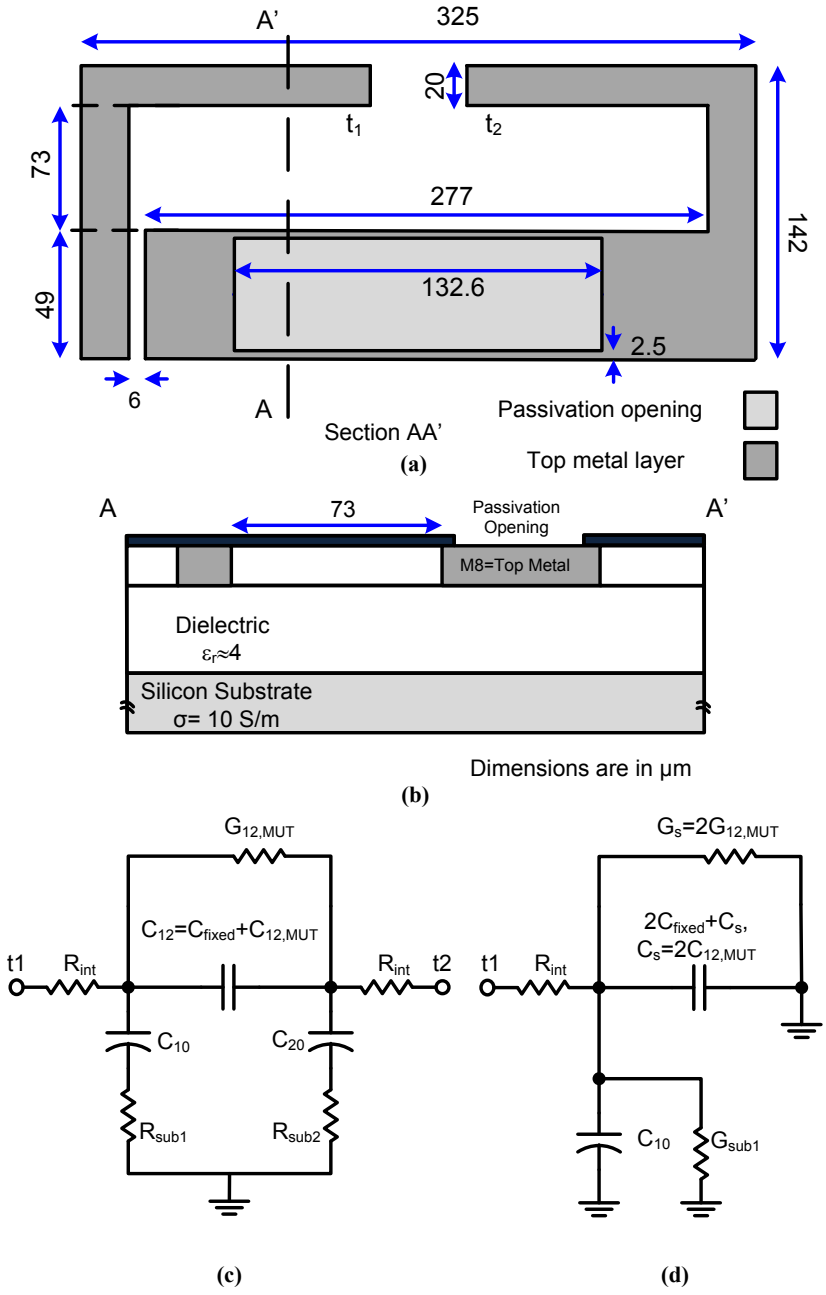


Figure 2.15: Sensor capacitor. (a) Top view of the sensor. (b) Cross section view (AA') of the sensor. (c) The differential electrical model seen between t1 and t2. (d) The single-ended version of the capacitor model. All dimensions are in micrometers.

permittivity detection.

A capacitor implemented on the top metal layer of a CMOS process with an area of 0.0461 mm^2, shown in Fig. 2.15(a) and (b), forms the sensing element. The 325 μm $\times$142 μm capacitor has the equivalent circuit model shown in Fig. 2.15(c). The MUT affects the electromagnetic (EM) fields between t1 and t2, with the admittance $Y_{12}(\omega)$ between t1 and t2 having a fixed capacitive component due to the direct parallel-plate capacitance between the capacitor's metal, C_{fixed}, a parallel plate capacitance to substrate, C_{10}, C_{20} and a fringing capacitance that changes according to the permittivity of the MUT, $C_{12,\text{MUT}}$. Loss components are present due to the substrate loss and MUT loss, which are modeled by R_{sub} and $G_{12,\text{MUT}}$, respectively. EM simulations show that the capacitor quality factor in air is approximately 4.7 at 10 GHz and degrades to 1.7 when loaded with an MUT with permittivity of 10 and $\tan\delta = 1$. While this sensor capacitor Q is lower than anticipated due to an error in the substrate loss estimation in the initial design phase, it is only a minor contributor to the total oscillator tank Q, and it does not have a significant impact on the overall system performance.

When the sensor is exposed to air, the fringing component consists only of $C_{12,\text{air}}$ due to air being lossless. After depositing a MUT with permittivity of $\varepsilon_r(\omega) = \varepsilon_r'(\omega) - j\varepsilon_r''(\omega)$, the fringing component changes to the parallel combination of $C_{12,\text{MUT}}$ and a conductive part, $G_{12,\text{MUT}}$. Neglecting the sensor interconnect resistance, R_{int}, the equivalent parallel- plate capacitance and conductance of the sensing element are approximately given by

$$C_{12,\text{MUT}} = \varepsilon_r'(\omega)\, C_{12,\text{air}} \;\&\; G_{12,\text{MUT}} = \omega\varepsilon_r''(\omega)\, C_{12,\text{air}} \tag{2.17}$$

Fig. 2.15(d) shows the equivalent half circuit model, where C_s is the effective

capacitance proportional to the real part of the material's dielectric constant, $C_s = 2\,\varepsilon_r'(\omega)\,C_{12,\mathrm{air}}$, and G_s is the effective parallel conductance modeling the effect of the material loss, $G_s = 2\,\omega\varepsilon_r''(\omega)\,C_{12,\mathrm{air}}$.

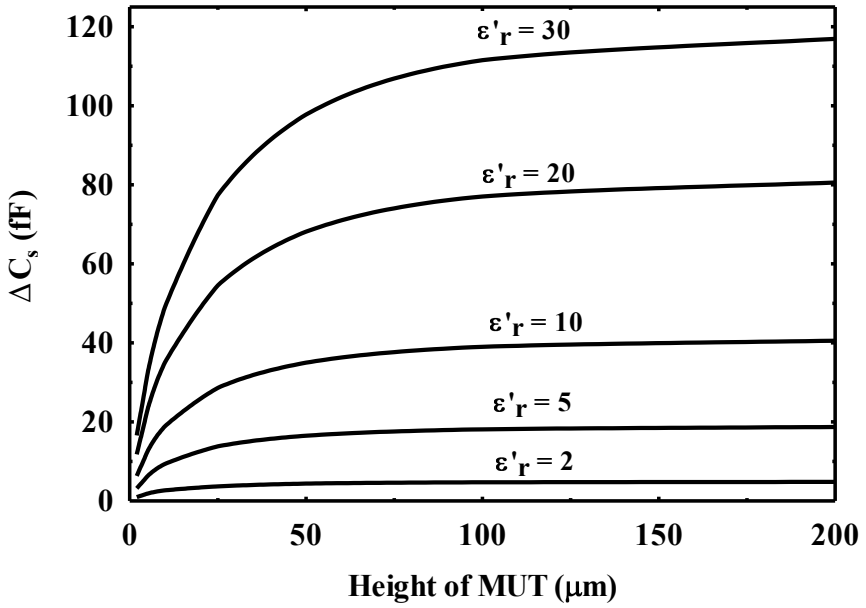


Figure 2.16: Sensing capacitance variations versus the deposited height of the MUT for five ε_r' values.

The capacitance C_s changes with ε_r' and with the height of the MUT deposited on top of the sensing capacitor [1]. EM simulations for the sensing capacitor were performed using Sonnet [29] where Fig. 2.16 shows the value of the sensing capacitance versus the MUT height for different values of ε_r' up to 30. The capacitance increases with MUT height until saturating for heights larger than 50 μm, which is considered to be the sensor EM field saturation height.

A more detailed expression for the sensor input capacitance is obtained from the total admittance at terminal t1, including the sensor interconnect resistance

$$Y_{t1} \cong j\omega C_o \frac{1 - R_{\text{int}} G_o}{1 + (\omega R_{\text{int}} C_o)^2} + G_o \frac{1 + \omega^2 C_o^2 R_{\text{int}}/G_o}{1 + (\omega R_{\text{int}} C_o)^2}, \tag{2.18}$$

where $G_o = G_{\text{sub}} + G_s$ and $C_o = 2\,C_{\text{fixed}} + C_{10} + C_s$.

Table 2.2: Sensor Capacitor Model Parameters in Air

C_{12}	7 fF
C_{10}	18 fF
C_{20}	55 fF
G_{sub1}	0.32 mS
G_{sub2}	1.15 mS
R_{int}	0.55 Ω

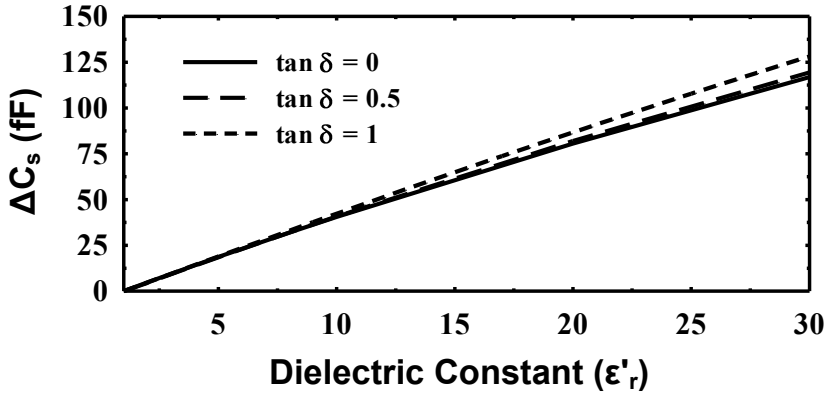


Figure 2.17: Sensing capacitance variations versus ε'_r of MUT for height 200 μm (above saturation height) at 10 GHz.

Equation (2.16) shows that in addition to the sensor capacitance terms, the sensor conductance can impact the total equivalent capacitance at t1 due to the interconnect

resistance term. R_{int} should be minimized in order to minimize the effect of the sensor conductance on its capacitance. As shown in Table 2.2, the R_{int} value of 0.55 Ω is achieved by using wide top-level metal connections. Fig. 2.17 shows that this allows for a nearly linear relationship between C_s and ε_r', with the loss tangent ($\tan\delta$) having only a small effect on the value of C_s for ε_r' less than 10.

2.3.2.2 Sensing VCO

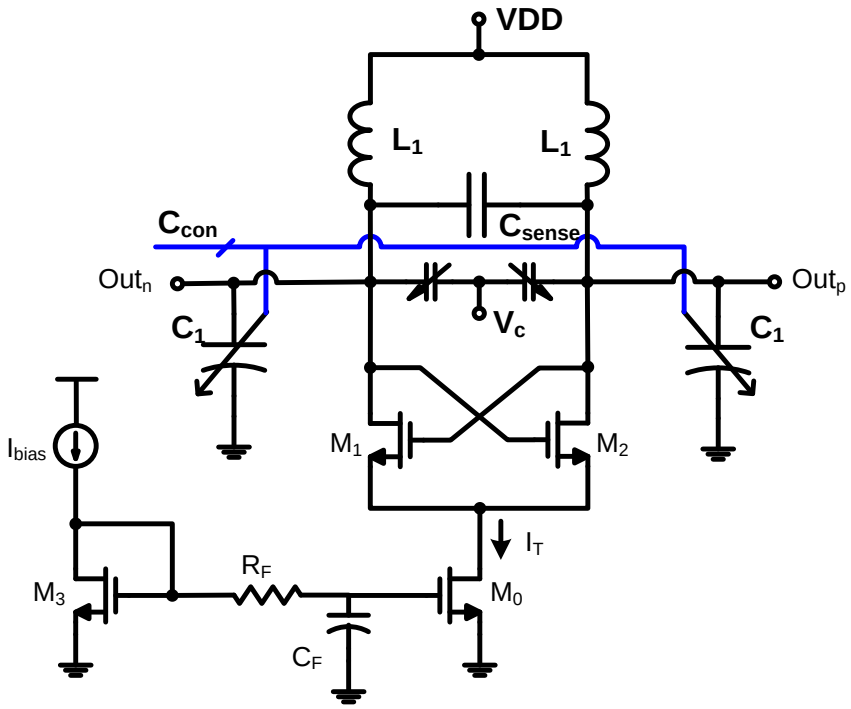


Figure 2.18: Simplified schematic of the nMOS cross-coupled sensing VCO.

Fig. 2.18shows a simplified schematic of the sensing VCO used to measure the capacitance change $C_s(\omega)$ due to the MUT deposition. The large intrinsic transconductance, with a relatively small parasitic capacitance of the nMOS cross-coupled transistors, allows for high-frequency operation at the nominal 1.2-V supply voltage.

In addition to the sensing capacitor, inductor L_1 and capacitor C_1 make up the oscillator's resonance tank. By applying the MUT, $C_s(\omega)$ changes and the frequency of oscillation shifts by a value of Δf. Assuming C_1 is much larger than $C_s(\omega)$, there is a linear relationship between $\Delta f/f_o$ and C_s the relative capacitance change for small frequency shifts

$$\frac{\Delta f}{f_o} \approx -\frac{1}{2}\frac{\Delta C_s}{(C_1 + C_s)} \approx -\frac{(\varepsilon_r' - 1)\, C_{12,\mathrm{air}}}{(C_1 + C_s)}, \tag{2.19}$$

where f_o is the resonance frequency in air.

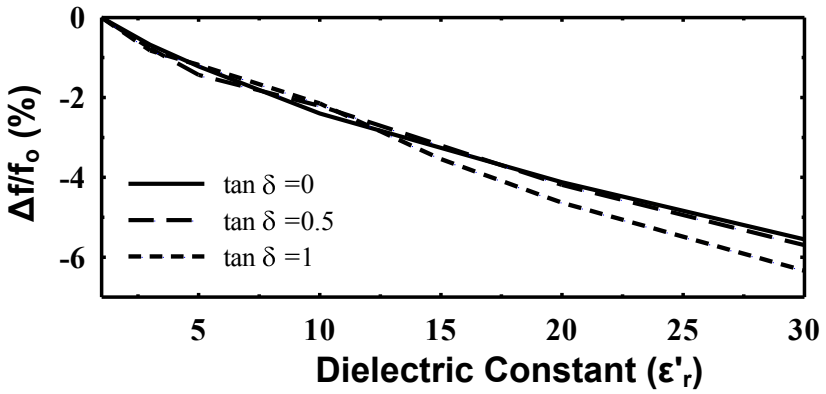


Figure 2.19: Percentage variation of the resonance frequency versus ε_r' for different values of $\tan\delta$ at a MUT height of 200 μm.

The simulation results of Fig. 2.19, which show the percentage variation of the VCO resonance frequency with ε_r' for different values of $\tan\delta$, verify this linear relationship and show only a small impact due to $\tan\delta$. Note that the material loss, or ε_r'', can affect the frequency shift due to two reasons, which are: 1) it can potentially change C_s (however, as shown in the previous section, ε_r'' has a small effect on

C_s) and 2) loss variations result in amplitude variations, which translate into frequency variations due to amplitude modulation to frequency modulation (AM–FM) conversion [30]. This AM-FM conversion is a nonlinear process, as shown in the VCO simulation results of Fig. 2.20. For small amplitudes up to around 0.45 V, the frequency is nearly constant versus the amplitude. However, as the amplitude further increases, the frequency decreases dramatically. Thus, to minimize the AM–FM conversion, the selected range for the VCO single-ended amplitude is designed below 0.45 V.

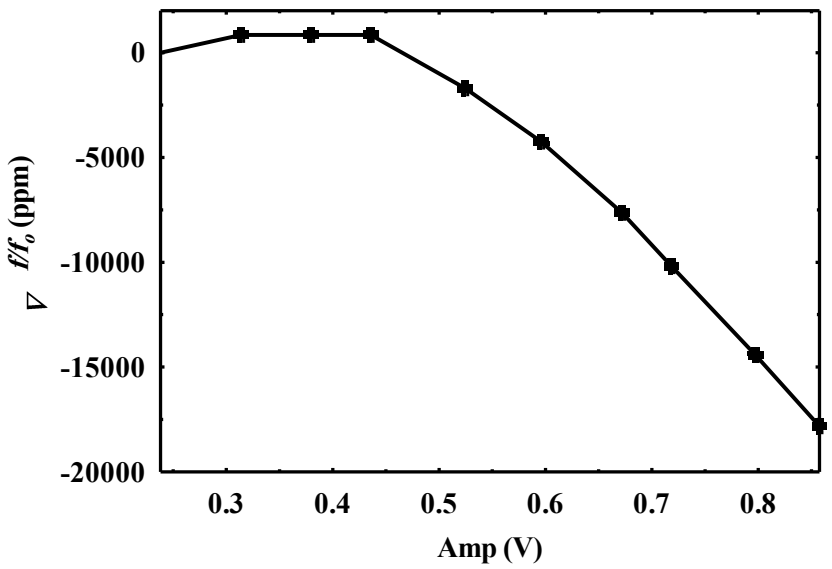


Figure 2.20: Percentage variation of the VCO output frequency versus the single-ended amplitude level.

2.3.3 Circuit Implementation

2.3.3.1 Sensor and Reference VCOs

In order to track the frequency drift of the sensing VCO due to environmental conditions and low-frequency noise, a reference VCO is also employed, as shown in Fig. 2.21(a). Since the frequency shift is measured as the difference in the oscillating frequency of both the sensing and reference VCOs, any correlated noise is filtered [19].While noise correlation is maximized with the sharing of as many elements as possible, with the best scenario involving the sharing of all VCO components, except the sensing and reference capacitors. In this case, the periodic enabling of the VCOs necessitates a high-frequency switch which degrades the tank quality factor considerably at 10 GHz. However, it is still possible to share the tail current source, which represents the primary source of flicker noise between the two VCOs with a low-frequency switch. Thus, the VCO noise contribution in the system frequency shift measurements is affected only by the non-common elements, which include the cross-coupled pair and the LC tank. It is worth mentioning that the applied MUT has a negligible impact on both the sensor and reference VCO tank inductance due to the virtually unity relative permeability of the materials under study. Moreover, any changes in the inductor's parasitic capacitance due to MUT application is minimized due to the 1 μm passivation layer between the MUT and the inductors.

The VCO phase noise should be minimized to enhance the sensor sensitivity, particularly at low-frequency offsets where flicker noise dominates. To achieve this noise reduction, the following design techniques are implemented.

1. The inductor quality factor is maximized at the operating frequency by employing a single-turn inductor using wide 4- μm-thick top metal (Al) tracks that are 5.75 μm from the substrate, resulting in an inductor quality factor

(Q_{L1}) of around 18. When varactor and sensor capacitor losses are included, the total tank Q degrades to 10 in the air and around 7 when loaded with an MUT with permittivity of 10.

2. A low-pass filter formed with R_F and C_F reduces the noise contribution of the bias transistor M_3.

In order to minimize the phase noise due to AM–FM conversion, the oscillator's bias current is adjusted to keep the single-ended oscillation amplitude around 0.45 V (Fig. 2.20). A peak detector, shown in Fig. 2.21(b), is connected to the VCO output to sense the amplitude level, which is used to control the amplitude. Table 2.3 summarizes the VCO transistor sizes and tank component values. Post-layout simulations show that the VCO operating near 10 GHz has a 7% tuning range, phase noise of -107 dBc/Hz at a 1-MHz offset, and 9-mA current consumption.

Table 2.3: Sizes of Transistors in VCO

M_0	480 μm/0.8 μm
M_1, M_2	22 μm/0.1 μm
M_3	80 μm/0.8 μm
M_4	768 μm/0.1 μm
L_1	220 pH
C_1	$\approx$ 1 pF

2.3.3.2 Frequency Divider

Fig. 2.22shows a detailed block diagram of the on-chip integer divider. To provide flexibility in reference clock selection, the integer divider has a programmable ratio from 256 to 504 with a step of 8. The divider is partitioned into current-mode logic (CML) stages, which offer high-frequency operation and superior supply noise

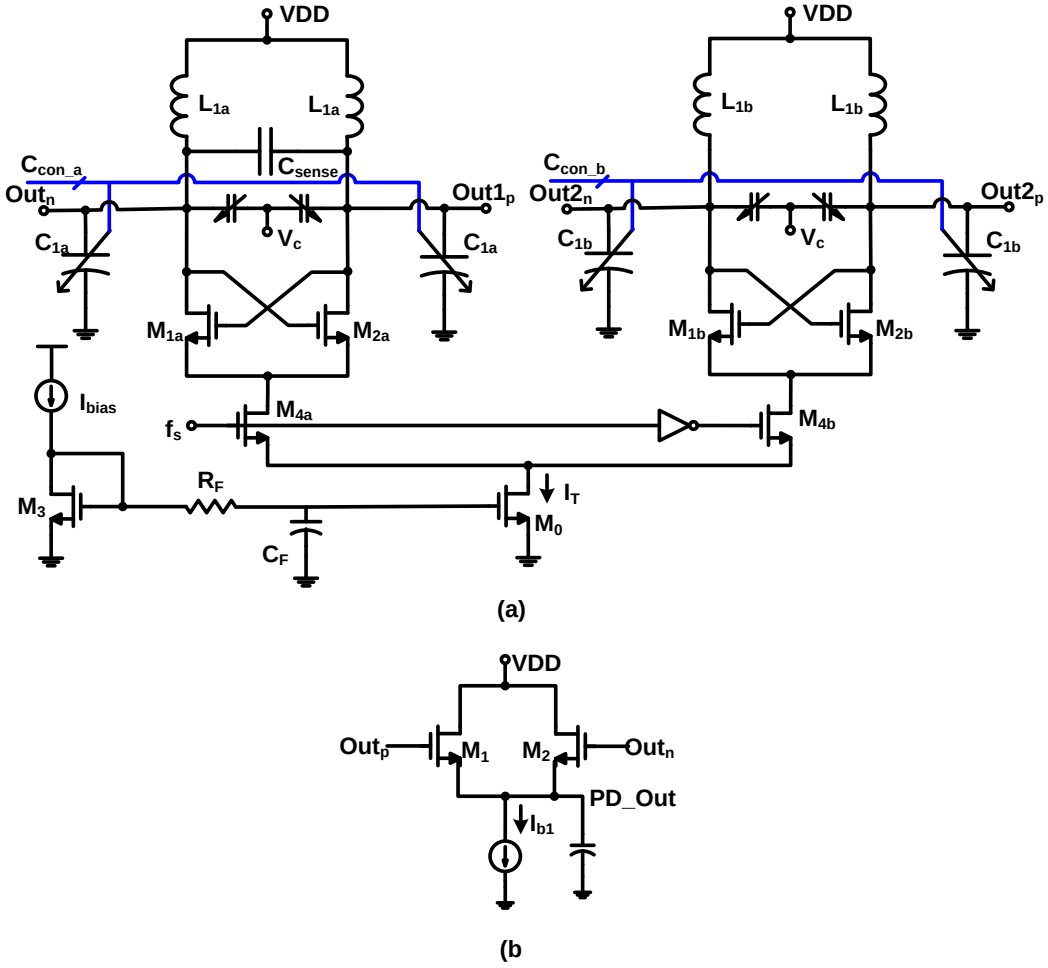


Figure 2.21: (a) Schematic of the shared bias VCO circuits (the sensing VCO and the reference VCO) with a common tail current source to increase correlated noise. (b) Peak detector schematic.

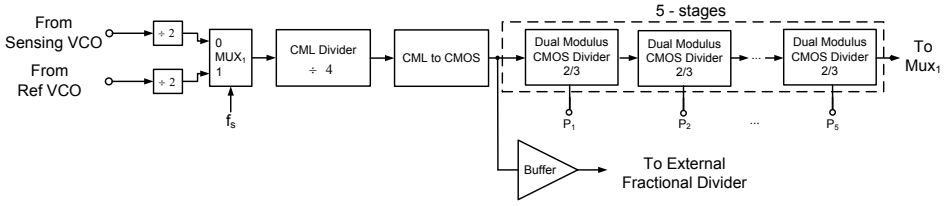


Figure 2.22: Integer frequency divider block diagram.

rejection, for the initial divide- by-8, followed by CML-to-CMOS conversion and the use of static CMOS circuitry to implement the remaining division in a robust and low-power manner. Two independent CML divide-by-2 blocks are utilized for the initial 10-GHz frequency division in order to provide sufficient isolation between the sensor and reference VCOs and also reduce oscillator loading. These initial dividers are ac coupled to the VCO for proper biasing and consume 2 mA each with an effective 12-GHz bandwidth. A MUX unit then selects which divided clock is placed in the loop and also serves as a buffer to drive a second CML divide-by-4 stage. As this second divider stage works near 1.25 GHz, it only consumes 0.3 mA. The CML-to-CMOS converter stage [31] drives both a buffer to the external fractional divider and the on-chip five-stage dual-modulus 2/3 divider [32] that provides a programmable division ratio from 32 to 63 with a step of 1.

2.3.4 System Integration and Test Setup

Table 2.4: Sensor Chip Power Consumption

Block	Power Consumption (mW)
VCO	10.8
High Frequency Dividers	7.2
PFD + CP	0.4
Output Buffer	3.6
Total	22

Fig. 2.23shows the chip microphotograph of the PLL-based dielectric sensor, which was fabricated in a 90-nm CMOS process and occupies a total chip area of 2.15 mm^2 . As detailed in Table 2.4, the overall chip power consumption is 22 mW, with the VCO and high-frequency dividers consuming the most power. An

open-cavity micro lead frame (MLP) $7 \times 7\,\mathrm{mm}^2$ QFN-48 package is used for chip assembly to allow for MUT deposition on top of the sensing capacitor. All electrical connections between the chip and the package lead frame are made via wire-bonding.

An off-chip commercial discrete fractional frequency divider (ADF4157) from Analog Devices is utilized in order to achieve high resolution in the frequency shift measurements. The external divider has 25-bit resolution, which allows for potential frequency shift measurements down to 6×10^{-4} ppm, considering the divide-by-8 on-chip CML divider. This implies that the system is not limited by the divider quantization noise, but rather by the system random noise discussed earlier. Fig. 2.24 shows the photograph of the printed circuit board (PCB) with the mounted sensor chip and the external divider. The sensor chip interfaces with the external divider with a buffered version of the on-chip CML divide-by-8 output at 1.25 GHz (Fig. 2.22) driven to the outer divider. Furthermore, the divided output signal at 25 MHz fed back to the CMOS chip to MUX (Fig. 2.10) that selects the PFD input based on the switching clock phase. Simple level-shifting interface ICs are used to condition the comparator's serial output bits to levels sufficient for the PC, which performs the digital filtering. The frequency shift measurement algorithm of Fig. 2.14 is performed automatically via a Labview program such that the MUT is deposited on top of the sensor, the external reference divider is adjusted with a successive-approximation procedure, and the corresponding frequency shift is measured directly.

2.3.4.1 System On-Board Integration

Organic chemical liquids, including methanol and ethanol and their mixtures, are applied to the sensor chip via a plastic tube fixed on top of the chip [1]. Due to the 1.2-mm tube diameter being comparable to the chip area and tube mechanical handling limitations, both the reference and sensing VCOs are covered by the MUT

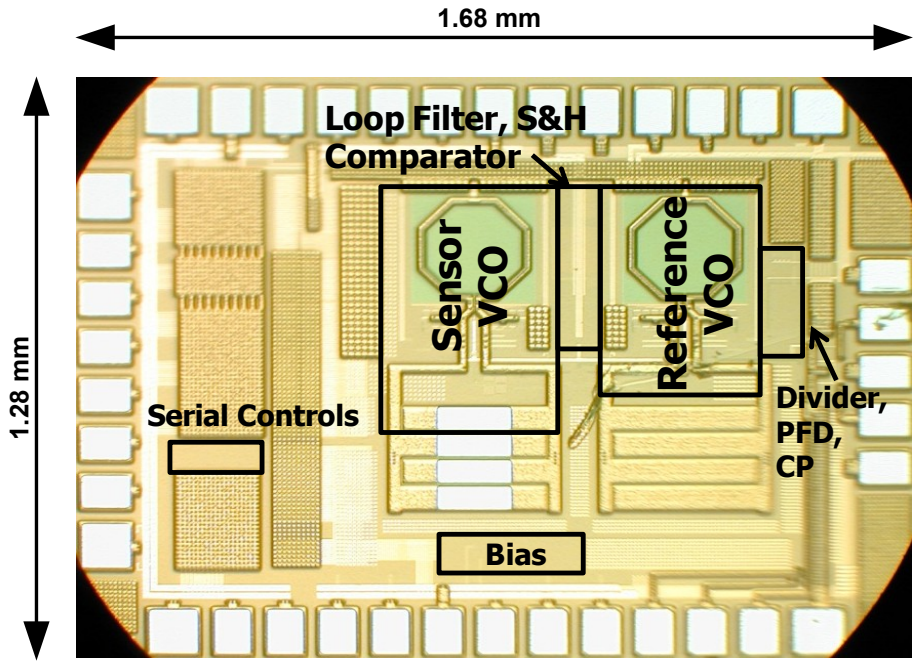


Figure 2.23: Microphotograph of the PLL-based dielectric sensor chip.

during testing. In order to avoid the effect of the MUT on the reference VCO, the metal capacitor in Fig. 2.23 is not attached to the reference oscillator. While this does result in a systematic offset between the VCOs, this is easily measured with the sensing capacitor exposed to air and later calibrated out. In order to control the volume of the material applied on the sensor chip, a Finnpipette single-channel micro-pipette is utilized to apply the liquid via the tube. After material application, the tube is capped to avoid evaporation. All measurements were performed with volumes less than 20 μL, which is sufficient to cover the sensor in excess of the saturation height due to the small sensor size.

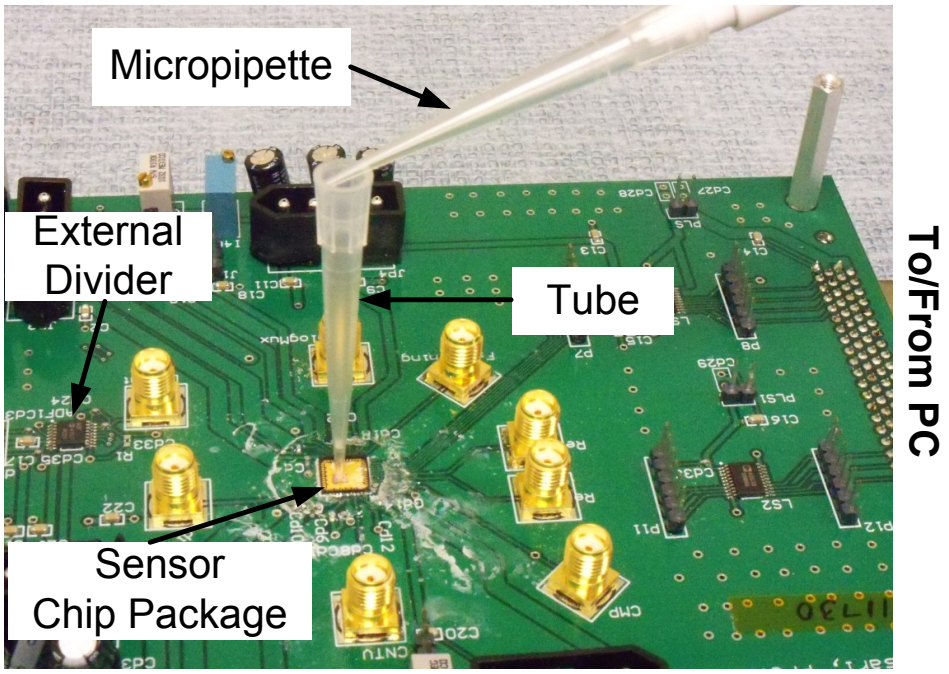


Figure 2.24: Photograph of the PCB with the chip, external divider, micropipette, and the MUT application tube indicated.

2.3.5 Experimental Results

This section discusses the fractional- PLL-based chemical sensor experimental results. First, key measurements of the PLL and system sensitivity are presented. Next, data is shown with the system characterizing organic chemical mixtures.

2.3.5.1 PLL and Sensitivity Characterization

The output spectrum and phase noise of the closed-loop PLL with the sensor VCO in the loop is measured at the output of the divide-by-8 CML block, as shown in Fig. 2.25 and 2.26, respectively. For the 1.3-GHz signal, reference spurs less than -60 dBc and a phase noise of -97 dBc/Hz at a 1 MHz offset are achieved. This phase noise converts to -79 dBc/Hz at a 1-MHz offset for the on-chip 10.4-GHz signal. As shown in Fig. 2.27, the PLL achieves a 640 MHz locking range between 10.04-10.68

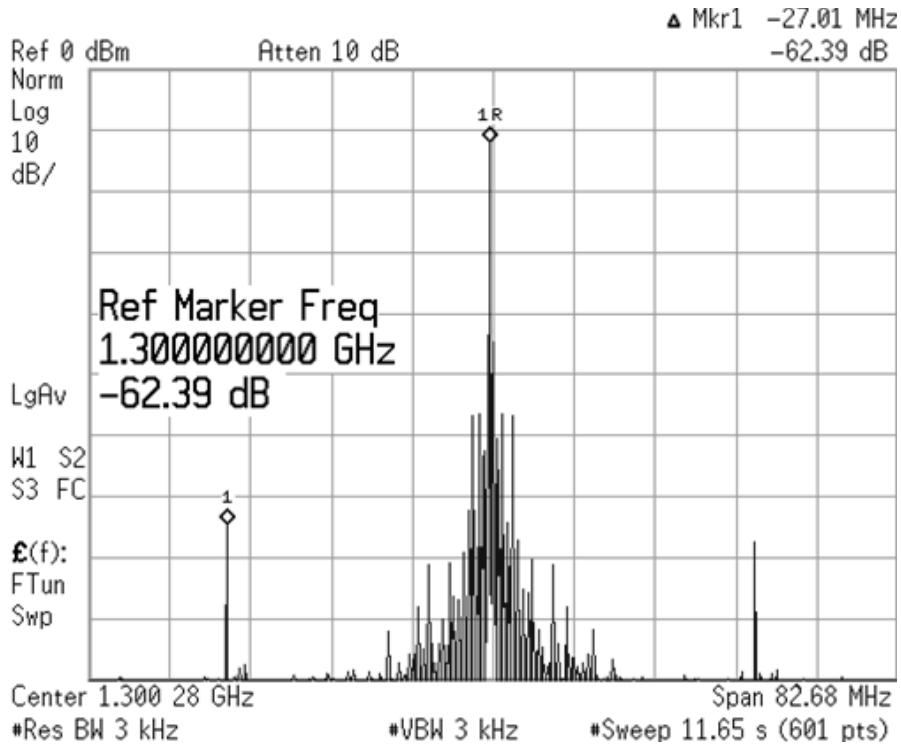


Figure 2.25: PLL output spectrum after CML divide-by-8 divider.

GHz and K_{vco} =885 MHz/V , at control voltage of 0.85 V, with the sensing VCO in the loop. Due to the absence of the sensor capacitor, the PLL achieves a 650 MHz locking range between 10.49–11.14 GHz and K_{vco} = 925 MHz/V , at control voltage of 0.85 V, with the reference VCO in the loop. Similar phase noise is achieved for both VCOs operating inside the PLL versus the control voltage.

In order to characterize the system noise level, the bang–bang divider control is set in open-loop, and a CDF of the average comparator output is produced by varying the external divider value, N_R. A switching frequency f_S = 1 kHz is employed in order to allow enough time for the PLL to settle with high accuracy. The results in Fig. 2.28 are fitted to a Gaussian distribution and a system noise sigma of 15 ppm

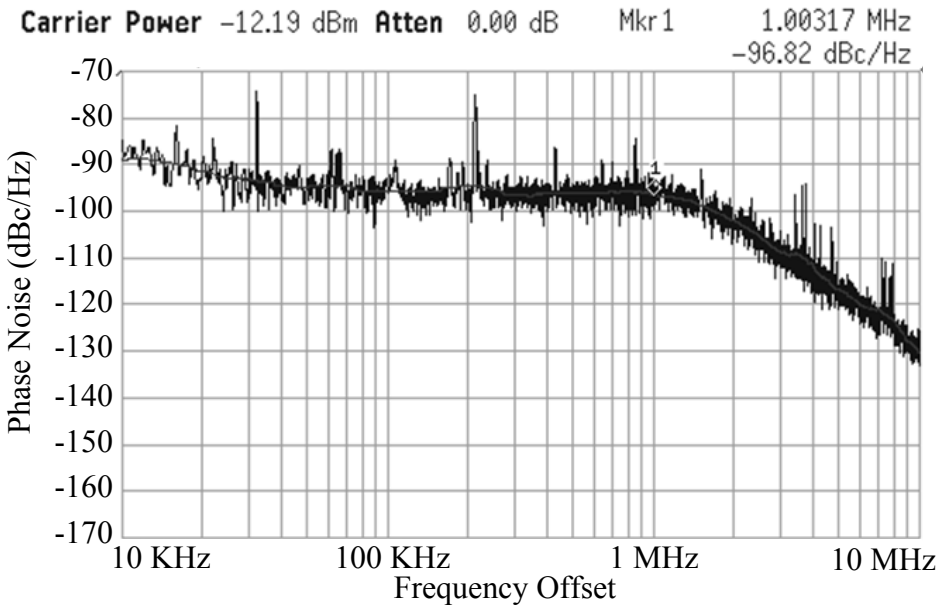


Figure 2.26: Reference VCO phase noise measurements after CML divide-by-8 divider.

is extracted. This noise value is very close to the 13 ppm predicted by previously discussed system simulations, indicating that the comparator noise is most likely currently limiting the system performance.

2.3.5.2 Sensor Calibration

As previously described in the Fig. 2.14 flowchart, the MUT is deposited on the sensor and the corresponding frequency shift is measured to determine the permittivity. Due to process variations, system offset, and K_{VCO} mismatches, the relationship between frequency shift and permittivity has to be calibrated for stable and accurate measurements. While (2.19) predicts an ideally linear shift in frequency with MUT ε'_r, the use of a higher order polynomial function allows additional degrees of freedom to calibrate for items such as K_{VCO} mismatches. A quadratic equation is used to

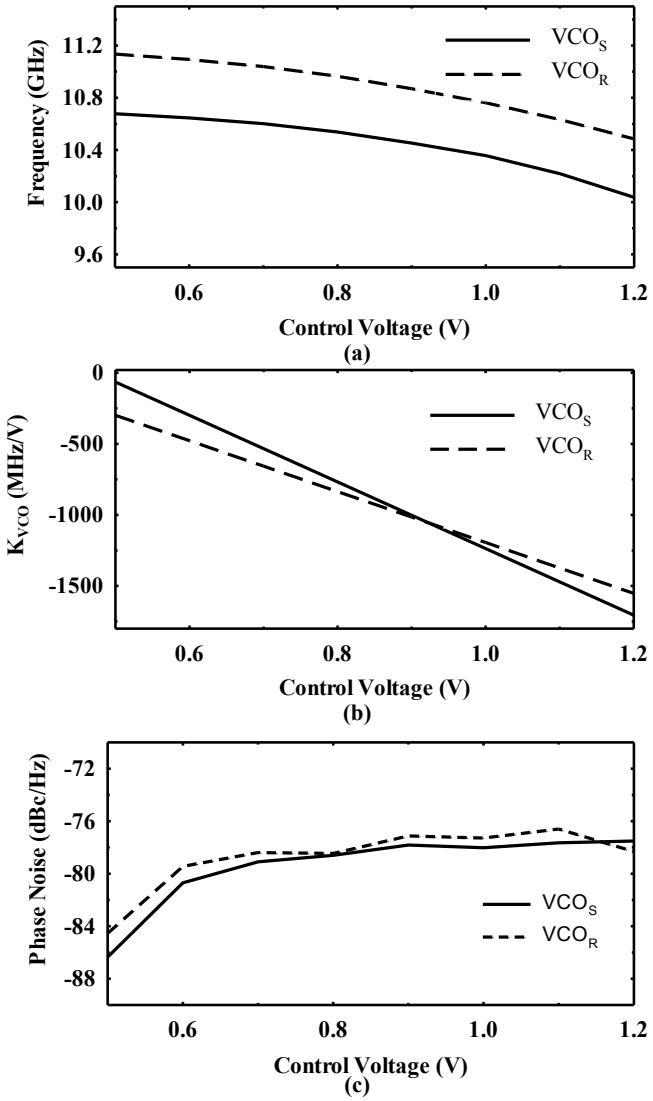


Figure 2.27: PLL measurements versus the control voltage with both reference VCO and sensor VCO. (a) VCO frequency. (b) K_{VCO}, and (c) Phase noise at a 1 MHz offset.

describe the frequency shift in megahertz as a function of the permittivity [1]:

$$\Delta f = a\ (\varepsilon_r' - 1)^2 + b\ (\varepsilon_r' - 1) + c, \tag{2.20}$$

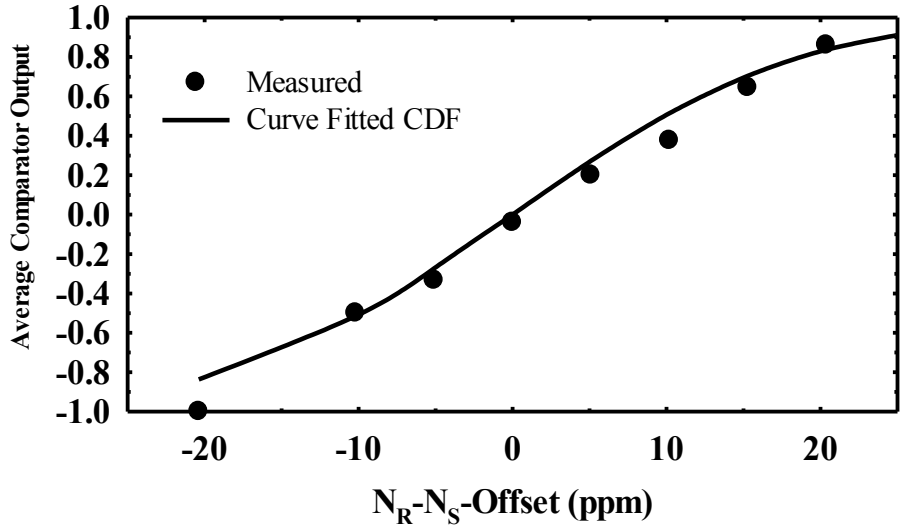


Figure 2.28: Measured average comparator output versus the difference in the divider values.

where a, b and c are the calibration constants. Note that the constant c represents the system offset mentioned in 2.3.1.2. Three calibration materials are required to determine these constants. In this work, air, pure ethanol, and pure methanol are used as calibration materials whose ε'_r at the testing frequency (10.4 GHz) are 1, 4.44–j2.12 ($tan\delta = 0.48$), and 7.93–j7.54 ($tan\delta = 0.95$), respectively [11]. Depositing each of these calibration materials on the sensor independently and measuring the induced frequency shifts allows extraction of a, b and c, which are found to be 0.0162, 19.9046, and 360.0808, respectively. During this calibration process, the comparator output is digitally filtered by averaging for 100–200 bits in order to ensure stable measurements. Fig. 2.29 shows how the measured frequency shift Δf versus ε'_r matches with the calibration curve.

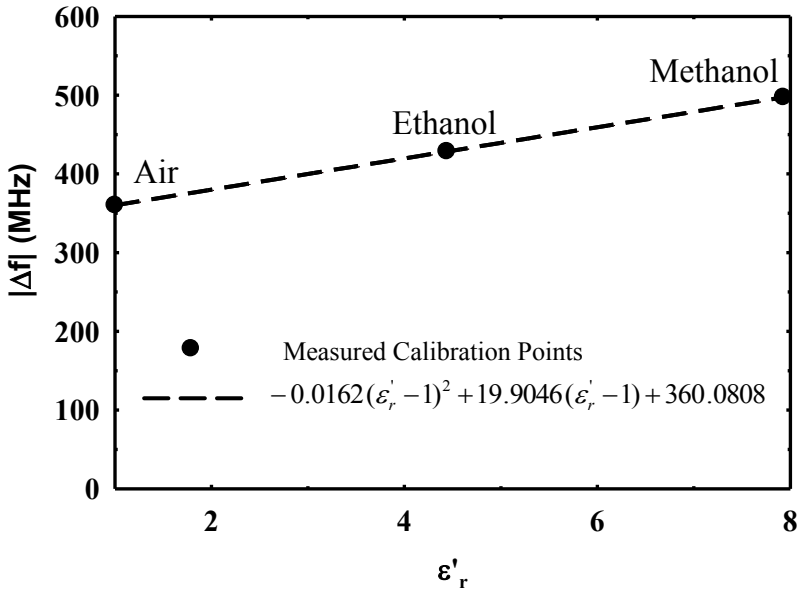


Figure 2.29: Fitted absolute frequency shift Δf versus ε_r' at the sensing frequency of 10.4 GHz with the calibration points indicated.

2.3.5.3 Mixture Characterization and Permittivity Detection

As a proof of concept, the system is used to detect the permittivity of a mixture of ethanol and methanol with several ratios of q and $(1-q)$, respectively, $0 \leq q \leq 1$. Mixture accuracy is ensured by preparation with high volumes using a micropipette with 1 μL accuracy. For example, with a q of 0.4 and a total volume of 500 μL, 200 μL of pure ethanol is mixed with 300 μL of pure methanol using the micropipette. 20 μL is then taken from the mixture and deposited on top of the sensor for detection.

For this case, the absolute value of the frequency shift is then measured and found to be 454.45MHz ($|\Delta f - c| = 94.38$ MHz). Using (2.20) and the values of a, b and c, the permittivity is then estimated to be 5.76. Repeating this procedure for other q values, Fig. 2.30(a) shows the frequency shift values Δf versus q, and Fig. 2.30(b) compares the measured ε_r' versus q with the theoretical Polder-van Santen mixture

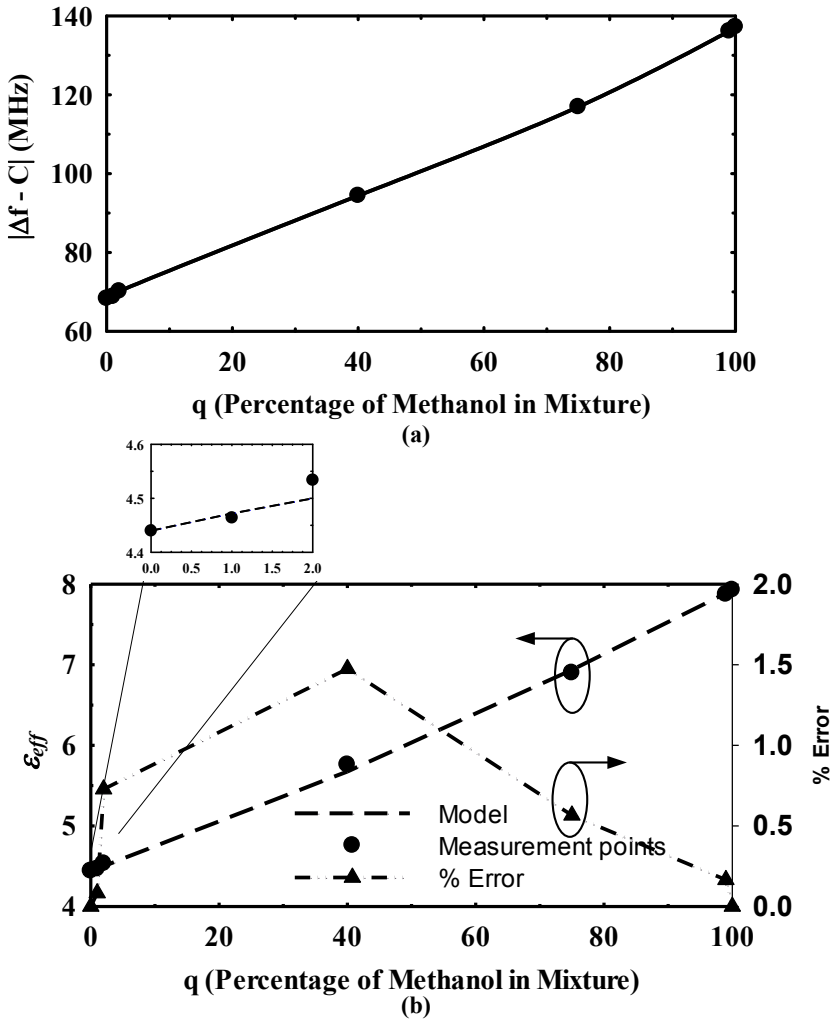


Figure 2.30: Measurement results of an ethanol–methanol mixture. (a) Frequency shift versus the concentration of methanol in the mixture. (b) Effective dielectric constant derived from the measured frequency shifts and compared to the model with $\nu = 2$ and permittivity percentage error.

model ($\nu = 2$) (2.9). The maximum difference between the measured and theoretical permittivity is less than 1.5%, as shown in Fig. 2.30(b). Note that the maximum error values are achieved for mixtures with comparable host and guest levels. Higher accuracy levels are achieved for more extreme ratios, with the sensor able to differen-

tiate mixture permittivities with fractional volume down to 1%. These measurements show that the detected permittivities fit quite well to the theoretical values and that the system can characterize mixtures at a high accuracy level.

Table 2.5 summarizes the performance and compares the results with prior work. This work achieves a higher level of integration and higher frequency measurement capabilities relative to the work of [23] and [34–36]. Compared to the system in [1], the presented fractional-N PLL-based sensor achieves a more than 2× improvement in permittivity error at comparable power consumption and CMOS integrated circuit (IC) area.

2.3.5.4 System Accuracy Limitations

Although the measured 15 ppm_{rms} system noise without material application (Fig. 2.28) converts to a 0.1% rms permittivity value from (2.20), several error sources contribute to the 1.5% maximum error observed between the measured and theoretical permittivity values. A discussion of these error sources follows, along with proposed solutions.

- K_{VCO} **mismatch:** While system performance is insensitive to K_{VCO} nonlinearity, K_{VCO} mismatch does impact the system error. The use of a higher order polynomial curve and additional calibration materials can reduce this error term.

- **Temperature dependency:** Since permittivity measurements are performed at room temperature without precise temperature control (while 20 °C permittivity values are used in the calibration procedure) any temperature variation will degrade sensor accuracy. A potential solution for future systems is to employ an accurate temperature sensor and integrated heater beside the sensing capacitor for temperature stabilization.

Table 2.5: Performance Summary and Comparison to Previous Work

	Sensor Read-Out Approach	Operating Frequency [GHz]	Area [mm^2]	Power Consumption [mW]	Permittivity Error [%]
Grenier [4]	S-parameters Lab Measurements	0.4-35	NA	NA	3[a]
Sekar [33]	Discrete Components[b]	4.5	NA	NA	2
Fractticcioli [34]	Discrete Components[c]	0.5-0.8	NA	NA	3
Saeed [35]	Network Analyzer	1,2 and 3	112×2.4[d]	NA	0.7-12
Saeed [36]	Network Analyzer	8	40×15[d]	NA	0.5
Laemmle [23]	Integrated Reflectometer PLL in 250nm SiGe BiCMOS	120-130	1.4	247.5	NA
Helmy [1]	Integrated PLL in CMOS 90nm[e]	7-9	2.5×2.5	16.5	3.5
This Work	Integrated PLL in CMOS 90nm[f]	10.4	1.6×1.28	22	1.5

[a] Error is reported at 25GHz,
[b] The system uses fractional-N PLL, micro-controller and ADC,
[c] The system uses PLL, peak detector and micro-controller,
[d] Sensor area only,
[e] Tunable reference oscillator is required,
[f] Off-chip fractional divider is used.

- **Mixing accuracy:** It is important to follow standard mixing procedures to ensure high measurement accuracy levels. Increasing the volumes mixed to obtain a given ratio can improve this.

- **Air/gas bubbles:** Any air or gas bubbles present in the material on top of the sensing capacitor will impact the measured permittivity. A more advanced microfluidics structure for material dispensing is a potential solution to this issue.

2.4 Cell Detector Cytometer Prototype

Label free cell detection and characterization has many benefits in early many medical and research fields. Early detection of cancer can be enhanced by detecting circulating tumor cells (CTCs). Each cell has certain electric properties depending on its size, its cytoplasm properties and its membrane properties. A flow cytometer can be used to differentiate between cells, but it requires high sensitivity and operation at different frequencies [37–39]. At very low frequencies less than 10 kHz, the membrane electrical properties (conductivity σ_{mem}, real permittivity ε'_{mem}) affects the effective impedance of the cell. Between 100 kHz and 50 MHz, the average properties of the cytoplasm (conductivity σ_p, real relative permittivity ε'_p) determine the effective impedance of the cell. At higher frequencies, the properties of inside of the cytoplasm affect the effective impedance. One parameter is used to describe the properties of the cytoplasm of cells is the Clausius–Mossotti factor $K_p(f)$ used in dielectrophoresis (DEP) to differentiate and identify the cells [40, 41]. $K_p(f)$ can be calculated by:

$$K_p(f) = \frac{(\sigma_p - \sigma_m) + j\omega\left(\varepsilon'_p - \varepsilon'_m\right)}{(\sigma_p + 2\sigma_m) + j\omega\left(\varepsilon'_p + 2\,\varepsilon'_m\right)} \approx \frac{-j\,(\sigma_p/\omega) + \left(\varepsilon'_p - \varepsilon'_m\right)}{-j\,(\sigma_p/\omega) + \left(\varepsilon'_p + 2\,\varepsilon'_m\right)}, \tag{2.21}$$

where σ_m is the conductivity of the medium ($\sigma_p >> \sigma_m$) and ε'_m is the real permittivity of the medium ($\sim 80\,\varepsilon_0$). The material is PBS with enough conductivity to preserve the cells alive.

A prototype flow cytometer was designed to determine the average properties of the cytoplasm of the cells to work between 100kHz and 100MHz. The microfluidic part was designed and fabricated by Po-Jung Huang and Prof. Jun Kameoka in Electrical and Computer Engineering Department at Texas A&M University, College Station. The microfluidic channel passed over two differential electrodes with separation of 20 μm between adjacent electrodes. The channel has three inlets and one outlet with 80 μm width, as shown in Fig. 2.31.

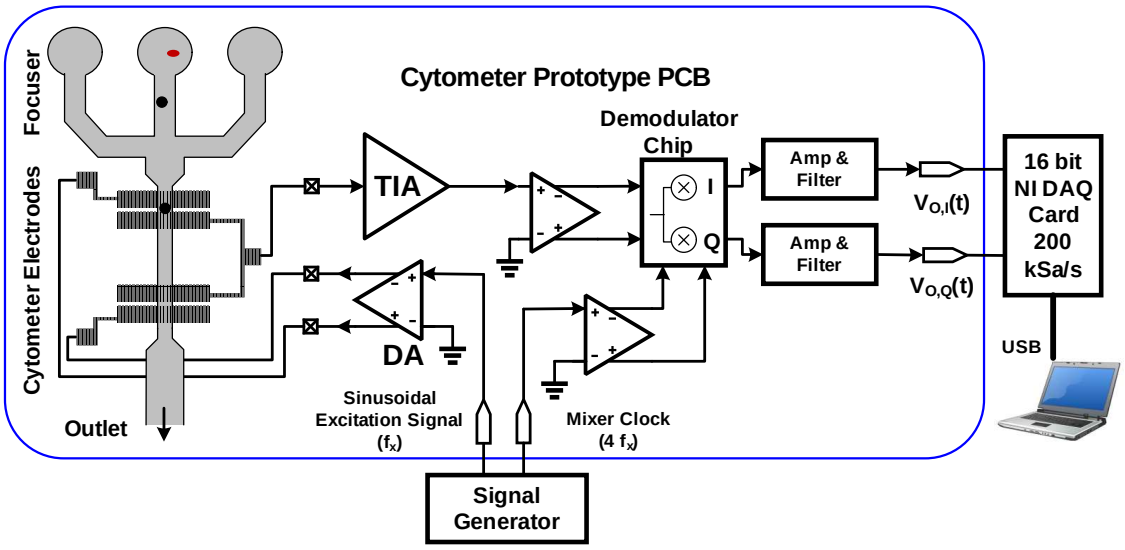


Figure 2.31: Block diagram of the flow cytometer prototype PCB.

The block diagram of the designed printed circuit board (PCB) is shown in Fig. 2.31. A signal generator is used to excite the electrodes by a sinusoidal signal and a sensing trans-impedance amplifier (TIA) is used to sense the differential

admittance and convert the sensed current to voltage. A modulator chip is used to convert the output of the TIA to baseband in-phase (I) and quadrature (Q) signals which are filtered and amplified. The amplifier bandwidth is more than 100 MHz, but the modulator chip can operate till 200 MHz clock ($\sim$ 50 MHz excitation signal). A 16 bit NI DAQ card is used to interface the I and Q output to be processed by the computer.

2.4.1 Cytometer Theory

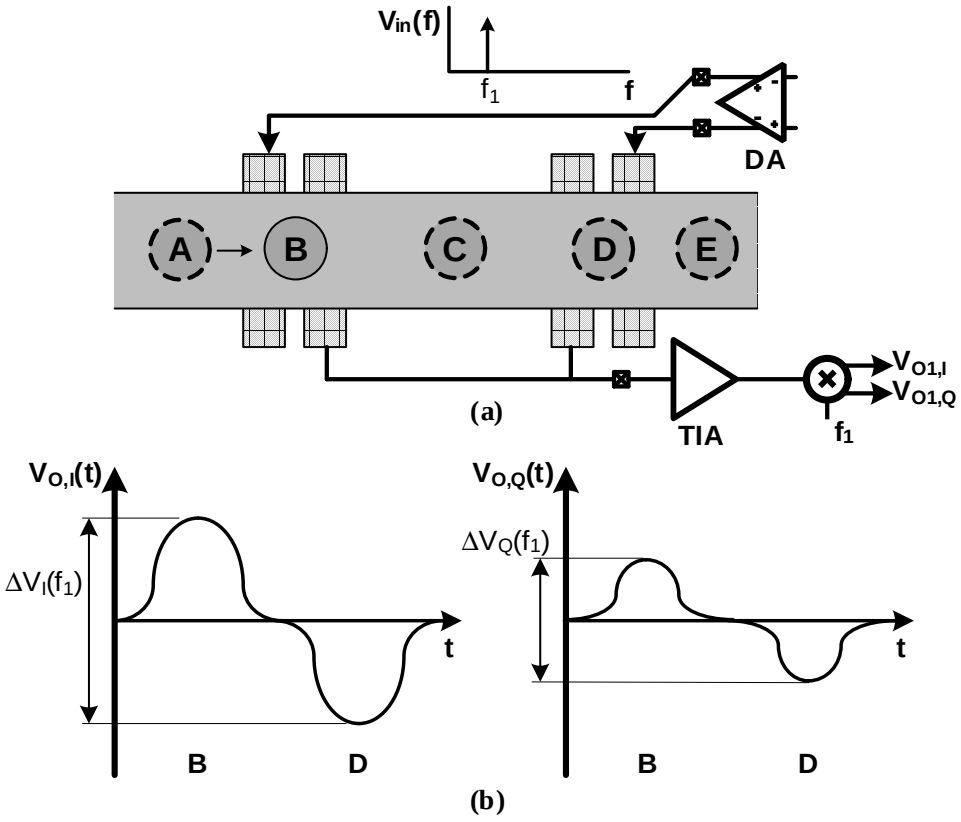


Figure 2.32: Theory of cytometer (a) Hypothetical block diagram with cell moving (b) Output of the cytometer after demodulation with time (I and Q outputs)

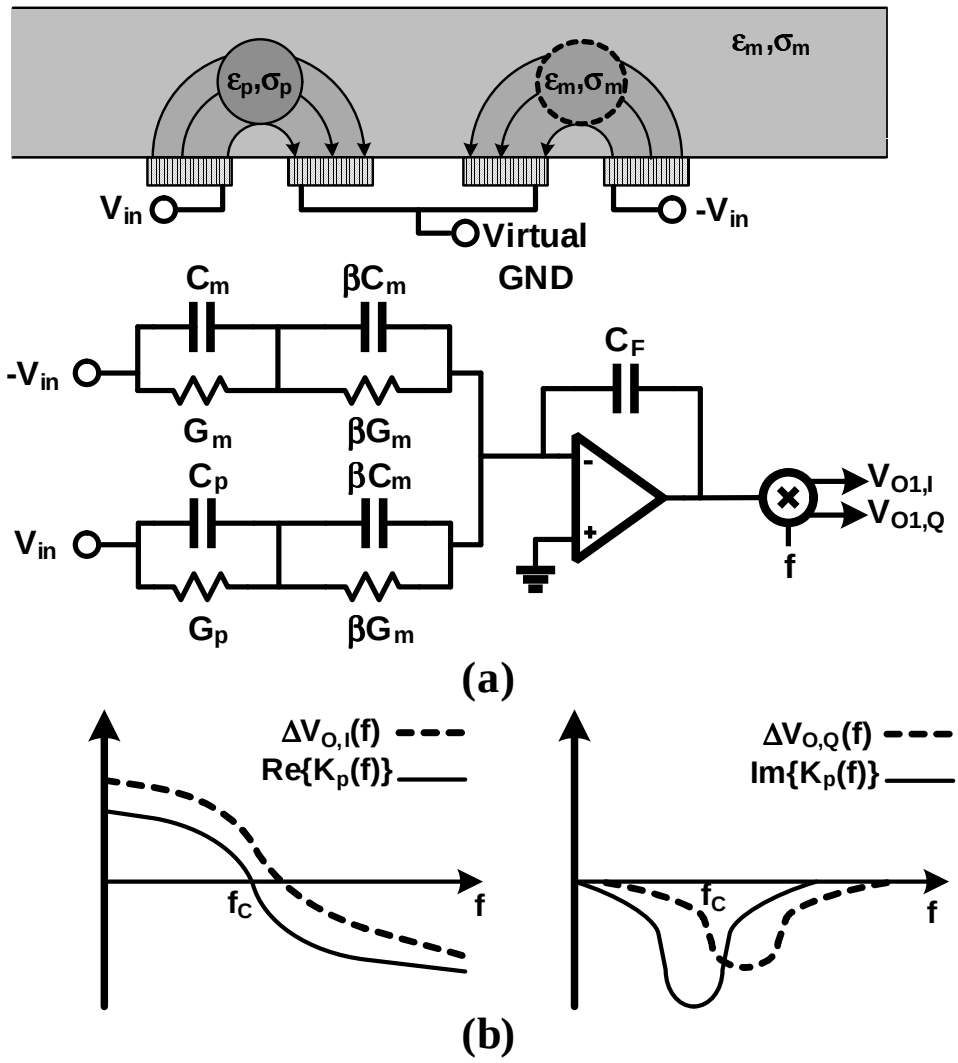


Figure 2.33: How to relate flow cytometer output to Clausius–Mossotti Factor $K_p(f)$, (a) flow cytometer electrodes and TIA, (b) Output and its comparison to $K_p(f)$.

The theoretical base of the operation of the cytometer is measuring the differential admittance while a cell passes over the differential electrodes. As shown in Fig. 2.32(a), the output voltage changes while the cell moves from position A to position E. The output is the difference between the voltages when the cell is at positions B and D, as shown in Fig. 2.32(b). The cell is modeled as a sphere with capacitance (C_p) and conductance (G_p) depending on the size of the cell and cytoplasm real

permittivity (ε'_p) and cytoplasm conductivity (σ_p), respectively. The surrounding of the cell is modeled by a tube that is in series the cell with capacitance ($\beta\, C_m$) and conductance ($\beta\, G_m$) which are proportional to real permittivity (ε'_m) and medium conductivity (σ_m), respectively, as shown in Fig. 2.32(a). C_m and G_m are the capacitance and the conductance of the same relative space of the cell but has medium electrical properties (ε'_m, σ_m). β is the ratio that between the admittance of the cell of the in-series medium to the admittance of the cell size but with medium properties. Therefore, β is only depending on the size of the cell and its position relative to the electrodes. The differential admittance ($\Delta Y\,(f)$) can be calculated by:

$$\Delta Y(f) = \frac{\beta\, Y_p Y_m}{(Y_p + \beta\, Y_m)} - \frac{\beta\, Y_m}{(1+\beta)} = \frac{\beta^2}{(1+\beta)}\, Y_m \frac{(Y_p - Y_m)}{(Y_p + \beta\, Y_m)}, \tag{2.22}$$

Since Y_p ($Y_p = G_p + j\omega C_p$) and Y_m ($Y_m = G_m + j\omega C_m$) are defined for the same dimensions:

$$\frac{\Delta Y(f)}{Y_m\,(f)} = \frac{\beta^2}{(1+\beta)}\, \frac{(\sigma_p - \sigma_m) + j\omega\left(\varepsilon'_p - \varepsilon'_m\right)}{(\sigma_p + \beta\,\sigma_m) + j\omega\left(\varepsilon'_p + \beta\,\varepsilon'_m\right)}, \tag{2.23}$$

$$\frac{\Delta Y(f)}{Y_m\,(f)} \approx \frac{\beta^2}{(1+\beta)}\, \frac{-j\,(\sigma_p/\omega) + \left(\varepsilon'_p - \varepsilon'_m\right)}{-j\,(\sigma_p/\omega) + \left(\varepsilon'_p + \beta\,\varepsilon'_m\right)}, \tag{2.24}$$

Comparing (2.24) to (2.21), $\Delta Y(f)$ has the same profile behavior as $K_p(f)$ but with β instead of 2 in the denominator. The complex output has same behavior as $K_p(f)$ but shifted to higher frequencies, as shown in Fig. 2.32(b) since $\beta << 2$.

The output of the TIA $V_{TIA}\,(f)$ is simply directly proportional to $\Delta Y(f)$ and can be calculated by:

$$V_{TIA}\,(f,t) = V_{in}\,(f)\, \frac{Y_{m0}\,(f)}{Y_F\,(f)} \beta\, \frac{-j\,(\sigma_p/\omega) + \left(\varepsilon'_p - \varepsilon'_m\right)}{-j\,(\sigma_p/\omega) + \left(\varepsilon'_p + \beta\,\varepsilon'_m\right)} g\,(t)\,, \tag{2.25}$$

where $V_{in}(f)$ is the input voltage that excites the flow cytometer, $Y_{m0}(f) = Y_m(f)\,\beta/(1+\beta)$ is the admittance of the medium measured using one electrode which can be found by calibration process, $Y_F(f) = 1/R_F + j\omega C_F$ is the admittance of the feedback of TIA where C_F is the feedback capacitance and R_F is the feedback resistance, and R_F is the function that determines the position of the cell versus time. By measuring the difference between position B and position D. The complex output at baseband $\Delta V_O^*(f)$ ($\Delta V_O^*(f) = \Delta V *_{O,I}(f) + j\Delta V *_{O,Q}(f)$) can be formulated as:

$$\Delta V_O^*(f) = 2\,A_0 V_{in}(f)\,e^{-j\phi}\frac{Y_{m0}(f)}{Y_F(f)}\beta\,\frac{-j\,(\sigma_p/\omega) + \left(\varepsilon_p' - \varepsilon_m'\right)}{-j\,(\sigma_p/\omega) + \left(\varepsilon_p' + \beta\,\varepsilon_m'\right)}, \tag{2.26}$$

where A_0 is the gain of the mixer, and is the phase difference between the excitation signal path and the modulator multiplying signal. The gain and phase are calibrated using capacitive micro-beads to have output $\Delta V_O(f)$ ($\Delta V_O(f) = \Delta V_{O,I}(f) + j\Delta V_{O,Q}(f)$) that is directly depending on the properties and calculated by:

$$\Delta V_O(f) = \beta\,\frac{\left(\varepsilon_p' - \varepsilon_m'\right)\left(\varepsilon_p' + \beta\,\varepsilon_m'\right) + (\sigma_p/\omega)^2 - j\,(1+\beta)\,\varepsilon_m'\,(\sigma_p/\omega)}{(\sigma_p/\omega)^2 + \left(\varepsilon_p' + \beta\,\varepsilon_m'\right)^2}. \tag{2.27}$$

2.4.2 System Simulations

The purpose of the system simulation of the cytometer is to verify its operation and to determine the practical Challenges and how to address them. The purpose of the cytometer system is to determine the electrical properties of the cell (ε_p', σ_p) to estimate the Clausius–Mossotti factor $K_p(f)$ variation with frequency using (2.21). Since the medium electrical properties (ε_m', σ_m) are known (0.1M PBS solution), the only unknown parameters in (2.27) are ε_p', σ_p and β. The parameter (β) is a

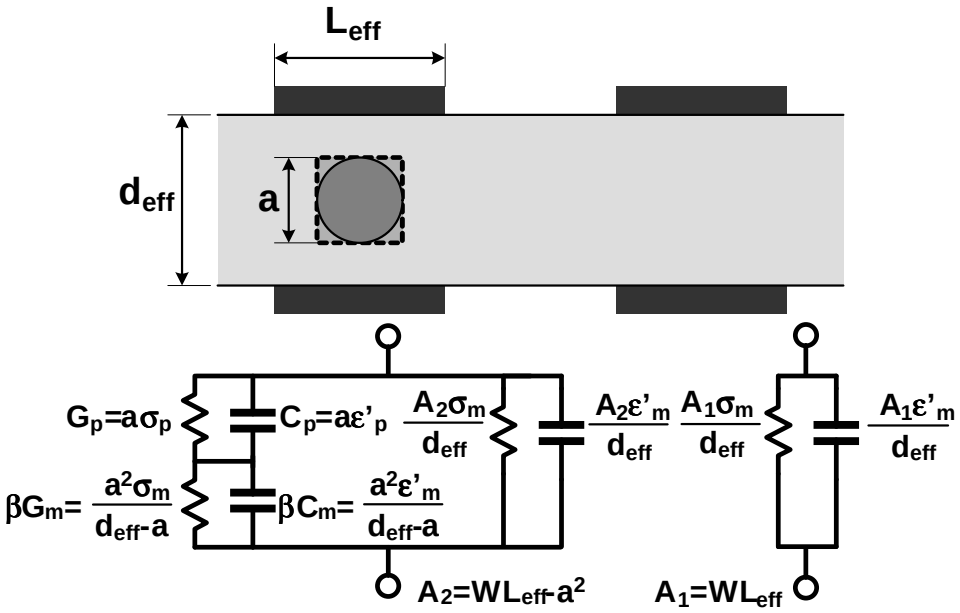


Figure 2.34: Simplified Cell Model in the channel.

scaling geometrical parameter which is nearly directly proportional to the size of the cell (unknown). To determine these three unknowns, three parameters are required to be measured by the cytometer for each cell. From (2.27), there are two outputs per frequency ($\Delta V_{O,I}(f)$ and $\Delta V_{O,Q}(f)$), but in reality, some of these values are not accurate enough due to the following issues: 1) phase adjustment and timing problems, 2) complexity of the dependence of output on cell electrical properties, 3) system noise and errors. To address the phase adjustment problem, one of the carrier frequencies should be very low frequency ($\sim$ 1MHz) to minimize the effect of both ε'_p and ε'_m. As a result, the output voltage has only a real part ($\Delta V_{O,I}(f_{1M})$) which is depending on the size of the cell or (β). This output voltage will be used as a normalization factor for the outputs at other frequencies to adjust the phase and gain. For the timing problem, a known micro-bead can be used for gain and delay calibration. The device is calibrated first and then β is determined using the

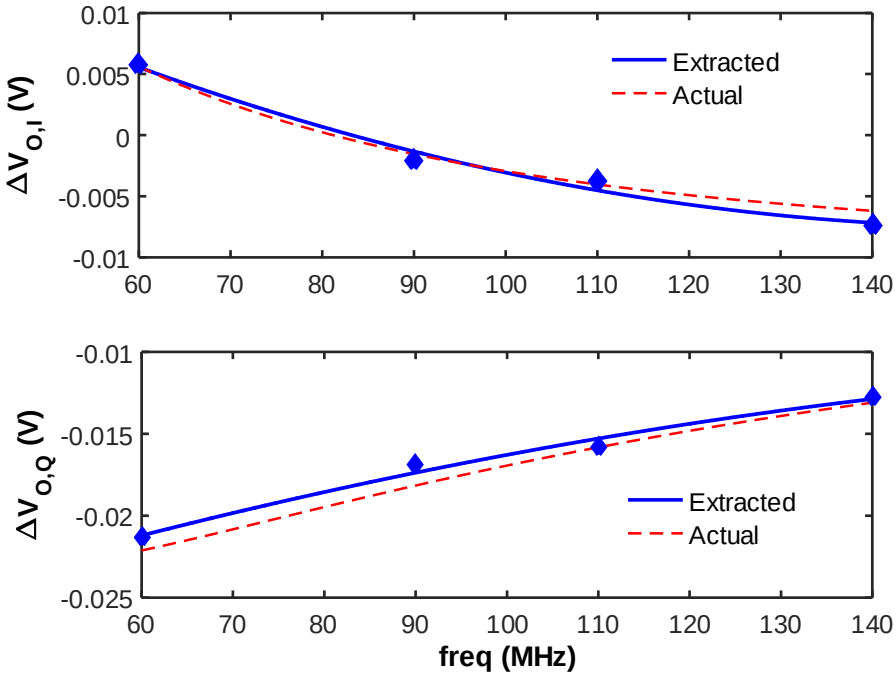


Figure 2.35: Simulink Results and comparison between the extracted output with the noise and the actual one

measured value $\Delta V_{O,I}(f_{1M})$.

To simplify the relation between the output and cell electrical parameters, the zero crossing frequency of $\Delta V_{O,I}(f)$ or $f_{c,Y}$ and the normalized value of $\Delta V_{O,Q}(f)$ at this frequency which can be easily measured are used to estimate $(\varepsilon'_p,\, \sigma_p)$. With the assumption that $\sigma_p >> \sigma_m$ and ε'_p and ε'_m are close, (2.27) can be used to estimate $f_{c,Y}$ and $\Delta V_{O,Q}(f_{c,Y})$ as follows:

$$f_{c,Y} \approx \frac{1}{2\pi}\sqrt{\frac{\sigma_p^2}{\left(\varepsilon'_m - \varepsilon'_p\right)\left(\varepsilon'_p + \beta\,\varepsilon'_m\right)}} \tag{2.28}$$

$$\frac{\Delta V_{O,Q}\left(f_{c,Y}\right)}{\Delta V_{O,I}\left(f_{1M}\right)} \approx -\sqrt{\frac{\left(\varepsilon'_m - \varepsilon'_p\right)}{\left(\varepsilon'_p + \beta\,\varepsilon'_m\right)}} \tag{2.29}$$

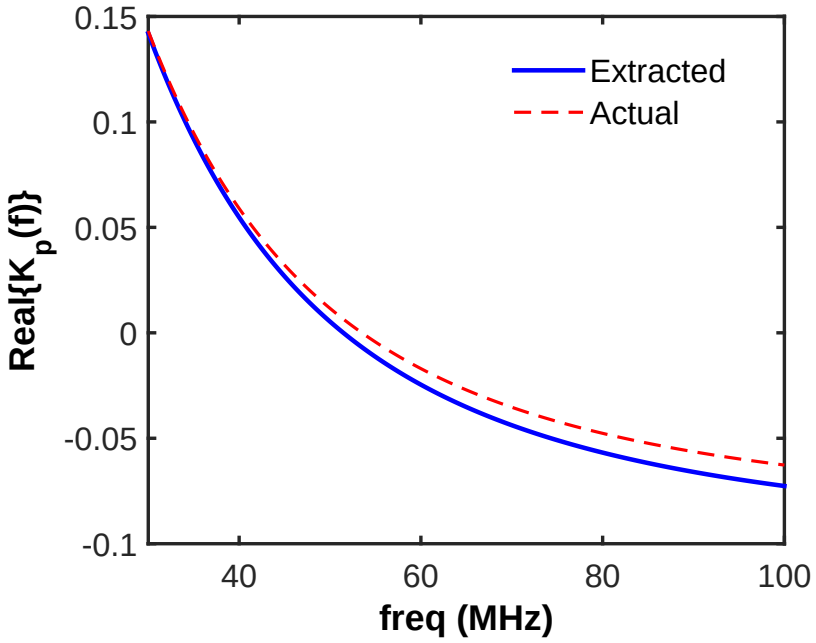


Figure 2.36: $Real\{K_p(f)\}$ using actual parameters and the extracted ones

To minimize the effect of the errors and noise, a simple least mean square (LMS) method is used on the output data to determine the best quadratic curve that fits the readings at the four carrier frequencies (other than 1MHz) and it is used to predict $f_{c,Y}$ and $\Delta V_{O,Q}(f_{c,Y})$.

A complete system simulation using MATLAB Simulink was built and tested on different cell sizes and cell parameters. The simulation target is to verify the above methodology for calibration and noise suppression. The simulation results are shown in Fig. 2.35, for the case where $a = 3\,\mu$m, $L_{eff} = 10\,\mu$m, $W = 80\,\mu$m, $d_{eff} = 14\,\mu$m, $\sigma_m = 0.019$ S/m (0.01X PBS), $\varepsilon'_m = 80\,\varepsilon_0$, $\sigma_p = 0.19$ S/m (10 times σ_m) and $\varepsilon'_p = 60\,\varepsilon_0$ defined in Fig. 2.34 with a flow rate= $2\,\mu$L/s. The simulation has five frequencies {1 MHz, 60 MHz, 90 MHz, 110 MHz, 140MHz} to have best accuracy around expected $f_{c,Y}$. Noise of the TIA is modeled by a white gaussian

noise source added to the output of the TIA.

The LPF bandwidth was chosen to be 29 kHz. The results show that the extracted output from the simulation in the presence of the noise will match well with the theoretical values output based on direct equations, as shown in Fig. 2.35. This implies that the extracted parameters will be close to the theoretical ones. A comparison between the real part of the Clausius–Mossotti factor $K_p(f)$ using theoretical parameters and the extracted ones from the simulation is shown in Fig. 2.36.

2.4.3 Measurement Results of Prototype

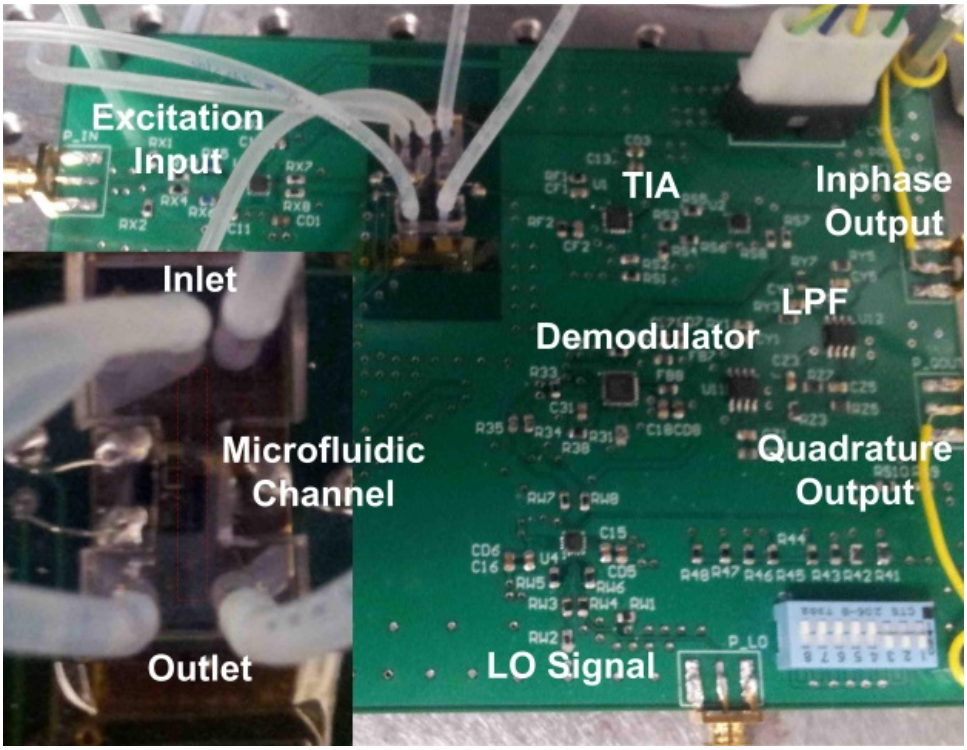


Figure 2.37: Photo of the prototype PCB.

A prototype was implemented to verify the concept and to have initial infor-

mation about the biomedical part before the integrated circuit implementation. A microfluidic was implemented above two sensing electrodes as shown in Fig. 2.37. The microfluidic structure was bonded directly the board using Aluminum bond-wires. This board can be used to measure the cell impedance at a single frequency which is excited externally. Discrete TIA and demodulator are used to down-convert the signal around the excitation frequency to baseband. A second order LPF with cutoff frequency 15kHz is used to filter the noise. The board can measure capacitance up to 500fF with a standard deviation of 0.2fF ($\sim$ 68 dB dynamic range) with input excitation frequency up to 60 MHz. Initial measurements on the prototype using two types of cells (cell 1: MCF-7 σ_p = 1.299 S/m, and cell 2: MDA-MB-231 σ_p = 1.168 S/m). The in-phase and the quadrature outputs at two frequencies (20MHz and 30MHz) are shown in Fig. 2.38. The outputs are normalized to 330 fF as a reference for the measurement. The initial measurements show that the responses are changing with frequency, and the two cells have different responses. Furthermore, it is clear from the graph that the variation of reading is small to identify the difference between the two readings. The error bars show the standard deviation of more than 500 cells.

2.5 Conclusion

The chapter introduces basic concepts of permittivity measurements techniques and presents the work done for two applications: 1) the integrated circuit high accuracy permittivity sensor, 2) the PCB-based flow cytometer.

A self-sustained fractional-N PLL-based CMOS sensing system is used for dielectric constant detection of organic chemicals and their mixtures at precise microwave frequencies. System sensitivity is improved by employing a reference VCO, in addition to the sensing VCO, which tracks correlated low-frequency drifts. A

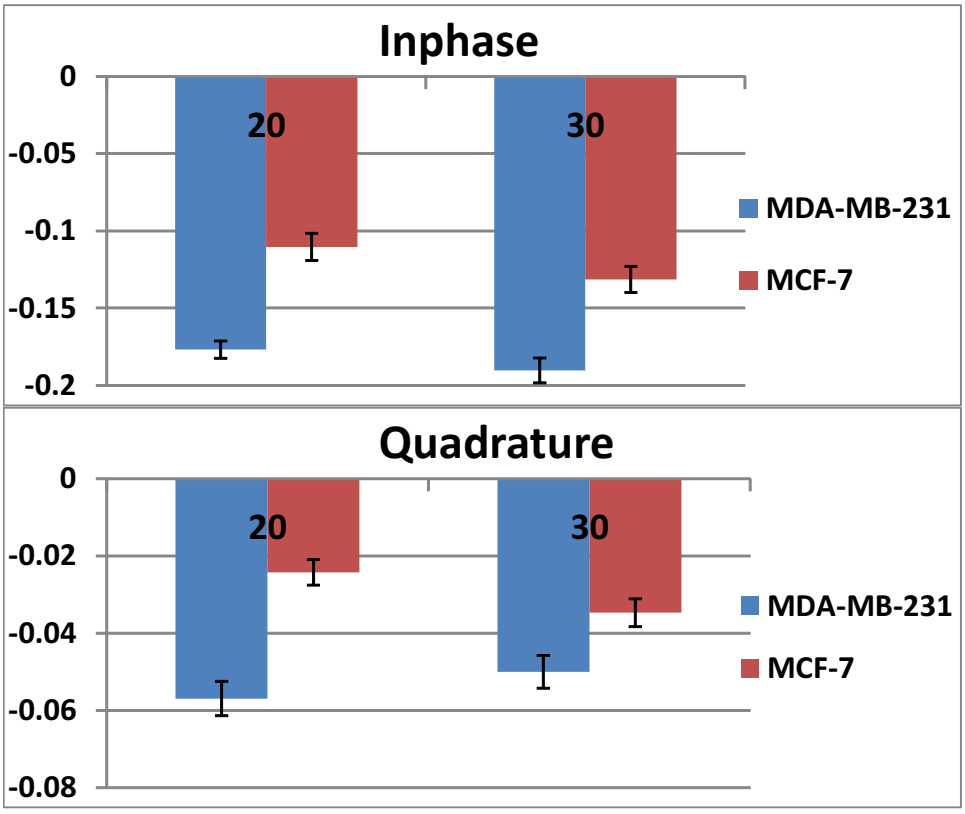


Figure 2.38: Measurements results where outputs are ratios to a reference capacitance for MDA-MB-231 and MCF-7 cells (for more than 500 cells).

simple single-step material application measurement procedure is enabled with a low-complexity bang–bang control loop that samples the difference between the control voltage with the sensor and reference oscillator in the PLL loop and then adjusts a fractional frequency divider. Binary mixture characterization of organic chemicals shows that the system was able to detect mixture permittivities with fractional volume down to 1%. Overall, the high-level of integration and compact size achieved in this work makes it suitable for lab-on-chip and point-of-care applications.

A proposed model for modeling the operation of flow cytometer is presented with a methodology to convert the results of the differential admittance measurements of the cells to the Clausius–Mossotti factor $K_p(f)$. A prototype PCB-based flow

cytometer is designed and tested to prove the capability to differentiate different cells (MDA-MB-231 and MCF-7 cells) using their response when passed through the microfluidic channel in the flow cytometer.

3. A WIDEBAND LOW POWER LC-DCO-BASED COMPLEX DIELECTRIC SPECTROSCOPY SYSTEM IN 0.18 μm CMOS

3.1 Introduction

Broadband dielectric spectroscopy (BDS) studies the dielectric properties of materials as a function of frequency to describe their types and quantities [42, 43]. BDS enables label-free, non-destructive, and real-time material characterization, which is a very valuable technique for numerous industrial, biological, and clinical diagnostics applications. The dielectric properties of materials, expressed by the complex relative dielectric permittivity ($\varepsilon_r^* \triangleq \varepsilon_r' - j\varepsilon_r''$), vary with frequency from lower than 1 mHz up to higher than 1 THz depending on the type of motion of the particles of the material. The radio frequency (RF) range is important since it can detect variations in the material properties down to the cell size and coarse intracellular variations. This has many biomedical applications such as cells detection [44], antibodies [45] or bacteria detection [46, 47].

Microwave frequencies can achieve higher resolution in determining intracellular permittivity variations [18, 38, 48]. At these frequencies, many liquid organic compounds have characteristic permittivity variation with frequency, that can be used for compound identification [49]. However, today's BDS instruments are not portable, very expensive, high power, and require large (100's of mL) sample volume. Integrated BDS platforms are highly desirable for many aspects: lower cost, smaller sample volume of the material under test (MUT), and smaller area of the sensor which can open new applications for BDS. Additionally, integrated low power BDS

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sensors have the potential to be used in hand-held devices or in emerging internet-of-things (IoT) applications.

There are two different approaches for measuring the MUT-loaded sensor admittance, namely amplifier-based BDS and oscillator-based BDS. In the amplifier-based approach, a single-tone voltage excitation signal is applied to the MUT-loaded sensor, and the current signal is measured as an amplitude and phase similar to an RF receiver front-end [16, 50]. This enables measuring both real (ε_r') and imaginary (ε_r'') permittivity across a wide frequency range. Because of the complexity of these systems, their power consumption is very high and they mostly rely on external high-resolution analog-to-digital converter (ADC) [16, 50]. More importantly, they usually use an external bulky excitation source (e.g., RF signal generator), because of the implementation challenges of a fully-integrated on-chip wideband pure sinusoidal signal source.

On the other hand, oscillator-based BDS platforms are simpler, self-sustained, and more power efficient [1, 20, 51]. The MUT-loaded sensor loads the oscillator circuitry and the sensor admittance shifts the frequency and the loop gain of the oscillator. In [1], the frequency shift due to an on-chip capacitor sensor is measured as a change in the control voltage of an LC voltage controlled oscillator (VCO) placed in a phase locked loop (PLL). However, this technique measures only the real permittivity (ε_r') and suffers from a narrow frequency range because of the LC-VCO. A wideband complex BDS platform using a ring VCO is proposed in [20]. It uses an amplitude-locked loop (ALL) technique to measure both ε_r' and ε_r'' through two frequency shift measurements. However, the poor phase noise performance of ring VCOs and the complex measurement procedures dramatically degrades the accuracy of the BDS system.

To address these challenges, this chapter presents an integrated chemical complex

dielectric spectroscopy system based on a wide band, low power, low noise LC-DCO. The proposed BDS system has three dual-band VCO cores to achieve a wide frequency range ($\sim$ 1-6 GHz). It can measure both $\varepsilon_r'(\omega)$ and $\varepsilon_r''(\omega)$ accurately and relies on a differential architecture, using sensor and reference oscillators, and correlated double sampling (CDS) scheme to minimize the impact of flicker noise and temperature variations on the sensor precision. The operation of the chemical sensor is verified by a prototype fabricated using a 0.18μm CMOS technology. The rest of the chapter is organized as follows: Section II provides the basic concept behind the proposed system. Section III presents the system analysis of the proposed BDS system. Section IV discusses the implementation details, while the measurement results of the prototype are shown in section V. Finally, the key contributions of this work are summarized in section VI.

3.2 Oscillator-Based Sensors

3.2.1 Capacitive Sensors

Dielectric constant or permittivity is an electrical property of materials that measures their ability to store electric energy in the presence of electric fields. Therefore, capacitive sensors are the most suitable to measure permittivity. The admittance of a parallel plate capacitors $Y_s(\omega)$ is directly proportional to permittivity and is calculated by:

$$Y_s(\omega) = j\,\omega\,\varepsilon_o\,\varepsilon_r(\omega)\,\frac{A}{d}, \tag{3.1}$$

where A is the surface area of the parallel plate, d is separation between plates, ω is angular frequency, ε_o is permittivity of free space, and ε_r is the relative complex permittivity. Since $\varepsilon_r^* \triangleq \varepsilon_r' - j\varepsilon_r''$, (3.1) can be simplified to:

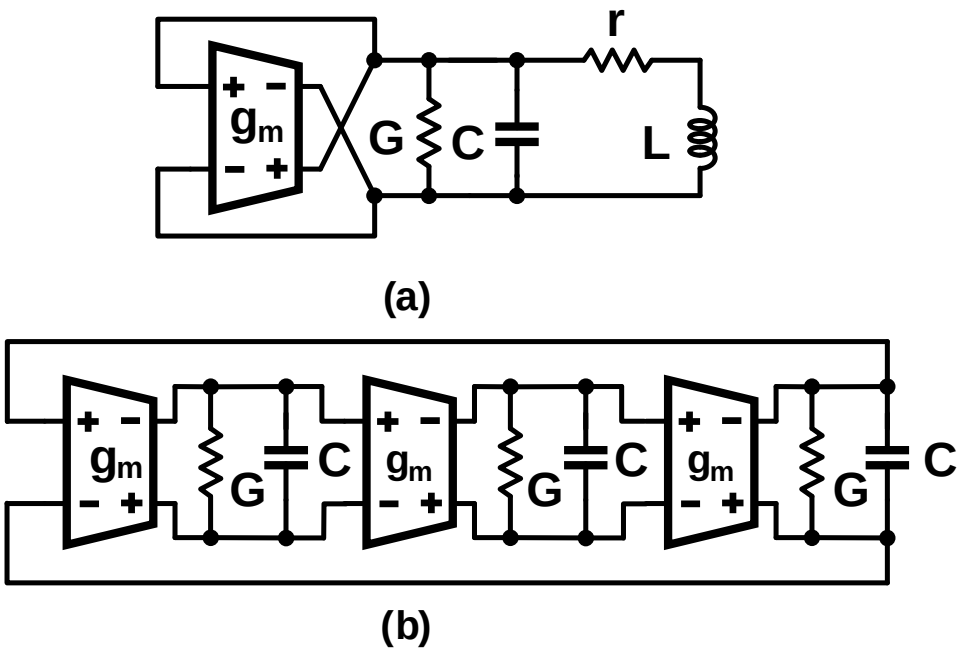


Figure 3.1: (a) LC-oscillator schematic where $C = C_d + C_t + C_s$, $G = G_d + G_t + G_s$ and r is series resistance of inductor, (b) three stages differential ring-oscillator schematic where $C = C_d + C_t + C_s$ and $G = G_d + G_t + G_s$.

$$Y_s(\omega) = j\,\omega\,C_s(\omega) + G_s(\omega) = \varepsilon_o \frac{A}{d}\left(j\,\omega\,\varepsilon_r'(\omega) + \omega\,\varepsilon_r''(\omega)\right), \tag{3.2}$$

where capacitance $C_s(\omega)$ is directly proportional to $\varepsilon_r'(\omega)$, and conductance $G_s(\omega)$ is directly proportional to $\varepsilon_r''(\omega)$. In this work, the admittance $Y_s(\omega)$ is measured by loading an integrated oscillator, in order to realize a simple self-sustained low power chemical sensor.

3.2.2 LC versus Ring Oscillator-Based Sensors

The frequency of an LC-oscillator depends on the value of its inductance and capacitance. Therefore, the tuning range of LC-oscillators is limited, while the phase noise performance depends on the quality factor (Q) of the resonating LC network.

The frequency of LC-oscillator $f_{osc,LC}$ seen in Fig. 3.1(a) can be calculated by:

$$f_{osc,LC} = \frac{1}{2\,\pi}\sqrt{\frac{1}{L\,(C_d + C_t + C_s\,(f_{osc}))} - \frac{r^2}{L^2}}, \tag{3.3}$$

where L is the differential inductance, C_t is the differential capacitance used for tuning, C_d is the effective differential capacitance of the active devices, $C_s\,(f_{osc})$ is the differential capacitance of the sensor at f_{osc}, and r is the series resistance with the inductance. The total capacitance is modeled by $C = C_d + C_t + C_s$, as shown in Fig. 3.1(a). The total differential conductance $G = G_d + G_t + G_s$ does not affect the frequency of oscillation, but it affects the loop gain at f_{osc}, where G_d models the differential conductance of the active devices, and the shunt conductance of the inductor, G_t models the parasitic differential conductance of the tuning capacitance with negligible variation, and G_s is the differential conductance of the sensor. The series resistances with capacitors are not considered since inductor loss is dominant at the required frequency range. The sensitivity of $f_{osc,LC}$ to C_s is determined by:

$$\frac{\Delta f_{osc,LC}}{f_{osc,LC}} = -\frac{\Delta C_s\,(f_{osc})}{2\,(C_d + C_t + C_s\,(f_{osc}))}. \tag{3.4}$$

Even though the sensitivity of f_{osc} to C_s is relatively low, the signal to noise ratio (SNR) of the sensor is still high due to the low phase noise of LC-oscillators. In [1, 18, 51], $\varepsilon'_r\,(\omega)$ is measured with high precision using an integrated LC-oscillator-based chemical sensors. However, they operate only in a narrow frequency band, as increasing the tuning capacitance C_t compared to C_s degrades the sensitivity and the precision of the sensor.

Ring oscillators can achieve very wide frequency operating range since the frequency varies with the current charging and discharging the capacitors. They also occupy a compact area, as a result, they are more suitable for sensor arrays than

LC except at very high frequency where the size of the inductor is significantly smaller [52]. In Fig. 3.1(b), a simplified schematic for a differential ring-oscillators with N delay stages is shown, where each stage has a resistive load and a full steered current operation [53]. The frequency of oscillation $f_{osc,ring}$ can be expressed as:

$$f_{osc,ring} = \frac{1}{2\,\pi} \frac{(G_d + G_t + G_s\,(f_{osc}))}{(C_d + C_t + C_s\,(f_{osc}))}\, tan\left(\frac{\pi}{N}\right). \tag{3.5}$$

Here, G_t is the differential conductance used for frequency tuning with parasitic differential capacitance. C_t and G_d models the differential conductance of the active devices. G_t controls the tuning range of the oscillator. The sensitivity of $f_{osc,ring}$ to C_s, and G_s is calculated by:

$$\frac{\Delta f}{f_{osc,ring}} = \frac{\Delta G_s\,(f_{osc})}{(G_d + G_t + G_s\,(f_{osc}))} - \frac{\Delta C_s\,(f_{osc})}{(C_d + C_t + C_s\,(f_{osc}))}. \tag{3.6}$$

This illustrates the coupled effect on ring oscillator frequency due to both C_s and G_s. Based on the fact that the amplitude is mainly depending on the variation of conductance only, an ALL was proposed by [20] to isolate the change in frequency due to ΔG_s from ΔC_s. By implementing this procedure, ring oscillators can be used to determine both $\varepsilon'_r\,(\omega)$ and $\varepsilon''_r\,(\omega)$, but with moderate accuracy. The sensor has a high sensitivity to C_s, as any small variations in C_s are translated to large variations in $f_{osc,ring}$, because C_d and C_t are small and comparable to C_s. However, ring-oscillators-based chemical sensors have poor signal to noise ratio (SNR) and relatively poor or moderate precision due to their poor phase noise performance. Furthermore, they considerably consume high power to operate at high frequencies.

3.2.3 Wideband LC-Oscillators

The frequency of the LC-oscillator can be tuned by changing inductance L or capacitance C_t as explained by (3.3) and (3.4). In 0.18 μm CMOS process used in this

work, $C_{t,max}/C_{t,min} \approx 3.15$, and $C_d + C_s \approx C_{t,min}$. Assuming fixed L, $f_{max}/f_{min} \approx 1.44$ (frequency tuning of $\pm 18\,\%$ around center frequency). The ratio of f_{max}/f_{min} depends mostly on the technology, since smaller feature size helps to minimize capacitances of the switches and the cross-coupled pair. Therefore, larger tuning range can be achieved for smaller feature size CMOS technology.

To achieve even wider frequency ranges, there should be a way to change L. Switched inductors were proposed to have large frequency steps providing wider tuning ranges, where the frequency in each range is controlled by changing C_t as in [54]. The main drawback in this topology is the added parasitics of the switch. Switch series resistance degrades the quality factor of inductor Q_L and hence considerably degrades oscillator phase noise. Additionally, switch off-capacitance decreases the self-resonance frequency of the inductor. Another solution to change the effective inductance seen by the oscillator is using two or more coupled inductors as seen in Fig. 3.2. By controlling the current direction flowing in one inductor, the effective inductance can be $L + M$ or $L - M$, where L is the self-inductance, and M is the mutual inductance between the two coupled inductors [55]. Since the trans-conductors used in this topology have high output resistance, the quality factor does not degrade.

Since minimizing phase noise is critical to achieving high SNR and minimize the perturbation of the output frequency reading, coupled inductors with coupled trans-conductors topology is the most suitable one to widen the frequency range of LC-oscillators. The oscillator has two modes of operation: low-frequency mode and high-frequency mode. In low-frequency mode, G_{m1} trans-conductor is ON and G_{m2} is OFF, while in high-frequency mode G_{m2} is ON and G_{m1} is OFF. In each mode, the tunable capacitance is used to change the frequency in such a way to have two overlapped ranges of frequency. Assuming $(L + M) / (L - M) \approx 2$, the

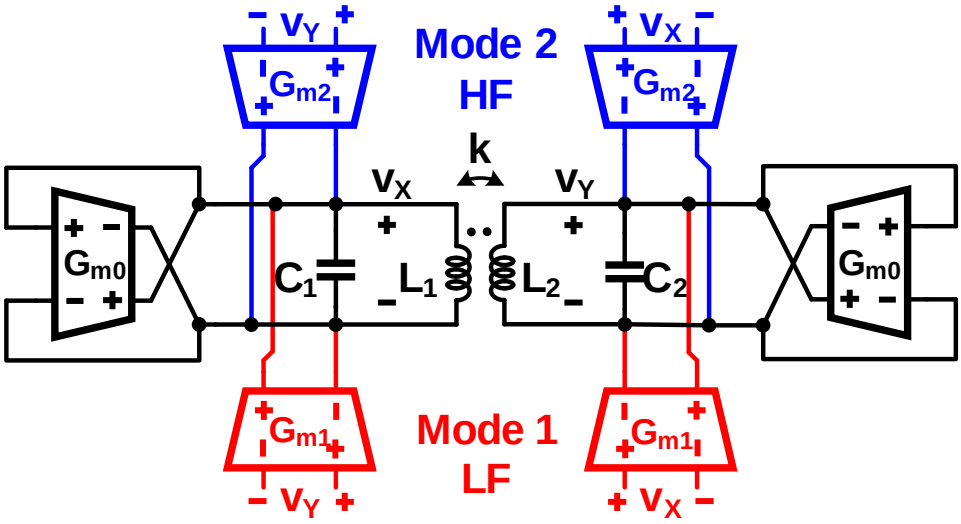


Figure 3.2: Dual mode oscillator has two modes of operation: 1) mode 1 for low-frequency range, 2) mode 2 for high-frequency range.

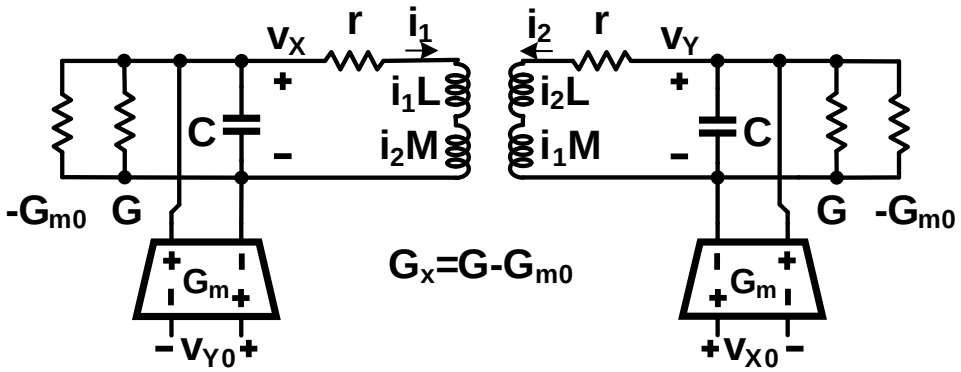


Figure 3.3: Model of the dual mode oscillator, where the transformer is replaced by the self-inductance L, the mutual inductance M, series resistance r and shunt conductance G_L as part of G ($G = G_L + G_d + G_t + G_s$).

total frequency range is nearly doubled such that $f_{max}/f_{min} \approx 2$ (frequency tuning of $\pm 34\,\%$ around center frequency).

Loop gain of the oscillator changes based on the mode of the oscillator. For a transformer with $L_1 = L_2 = L$, loss of L_1 and L_2 can be modeled by series resistances

r_{L1} and r_{L2}, respectively, ($r_{L1} = r_{L2} = r$), and shunt conductances G_{L1} and G_{L1}, respectively, ($G_{L1} = G_{L2} = G_L$), modeling the substrate loss for the transformer. G_{L1} and G_{L2} are added to G_{d1}, G_{t1} and G_{s1}, and G_{d2}, G_{t2} and G_{s2} to form G_1 and G_2, respectively, and is shown as G in Fig. 3.3 ($G_1 = G_2 = G$). The transformer is modeled by its mutual inductance M in series with the self-inductance L on each side. Using nodal analysis and superposition, the open loop gain $L(s)$ defined from v_{X0} to v_X or from v_{Y0} to v_Y is calculated by:

$$L(s) = \frac{s\,M\,G_m}{\left(1 + (s\,L + r)\,(s\,C + G_x)\right)^2 - s^2 M^2\,(s\,C + G_x)^2}, \tag{3.7}$$

where G_m is the differential trans-conductance from v_X to v_Y and vice versa, and $G_x = G - G_{m0}$. G_{m0} is the differential cross-coupled transconductance at each node v_X and v_Y. Assuming G_x is negligible and $G_{m0} \approx G$, the frequency of oscillation is determined by the Barkhausen condition as:

$$\omega_{osc} = \frac{1}{\sqrt{C\,(L \pm M)}}\sqrt{1 \pm \frac{r^2 C}{2\,M}}, \tag{3.8}$$

and the gain condition for oscillation is satisfied by:

$$G_m \geq \frac{C\,r}{M}\,\left(1 - \omega^2\,L\,C\right) \approx \frac{\pm C\,r}{L \pm M}. \tag{3.9}$$

From (3.8), the actual frequency of oscillation has two values: one low frequency close to $\omega_L = 1/\sqrt{C\,(L + M)}$, and one high frequency close to $\omega_H = 1/\sqrt{C\,(L - M)}$. The value of G_m required at ω_L is positive, while at ω_H is negative with nearly double the magnitude. Since this oscillator is essentially two coupled oscillators, coupled in-phase in low-frequency mode and out of phase at high-frequency mode, the phase noise performance is better than single oscillator by a factor of 3 dB. To cover a very wide frequency range of 1-6 GHz, three dual-band oscillators were used with

three different capacitive sensors. The three capacitors are all subjected to the same MUT, and only one oscillator is working at a time. Since each oscillator has a different sensitivity, calibration is required to link the results of the three sensors together.

3.2.4 Proposed System for Complex Permittivity Measurement

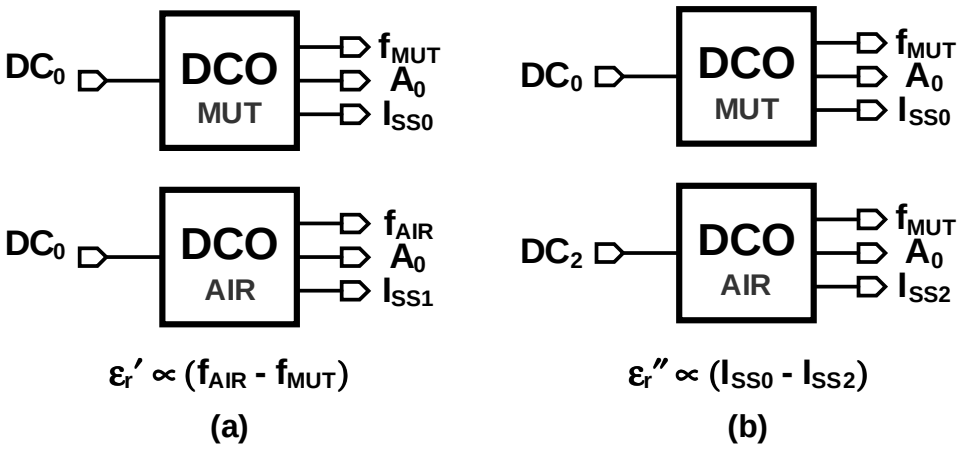


Figure 3.4: (a) Model for reading ε_r' at same input digital control and same amplitude but different frequencies. (b) Model for reading ε_r'' at same frequency and amplitude but different input digital control.

The proposed system to measure the complex permittivity of MUT is based on a dual-band LC digitally controlled oscillator (DCO) architecture operating in an open loop status. Measuring capacitance C_s is indicative to ε_r', and measuring conductance G_s is indicative to ε_r''. To measure C_s at certain frequency f_{MUT}, two identical oscillators are used where one of them has the sensor capacitor loaded by MUT, while the other one is left in the air, as shown in Fig. 3.4(a). DC_0 is the control word for the capacitor bank of the DCO for both oscillators to have fixed C_t and C_d in (3.3), such that the oscillator with MUT oscillates at f_{MUT}. For better

stability of the frequency, an ALL is used to have constant amplitude A_0 for both oscillators. From (3.2) and (3.4), $\varepsilon'_r(f_{MUT})$ is calculated at fixed C_d and C_t by:

$$\varepsilon'_r(f_{MUT}) - 1 \approx \frac{2\,C_{total}}{C_{s0}}\left(\frac{f_{AIR} - f_{MUT}}{f_{MUT}}\right), \tag{3.10}$$

where f_{AIR} is the frequency of oscillation in the air, while f_{MUT} is the frequency of oscillation with MUT, C_{total} is the total capacitance to achieve f_{MUT} ($C_{total} = C_d + C_t + C_{s0}\,\varepsilon'_r(f_{MUT})$), C_{s0} is the capacitance of the sensor in air.

Measuring conductance using an LC-oscillator is challenging, since it does not affect the frequency. However, the conductance affects the loop gain of the oscillator and the amplitude of oscillation. Assuming a current limited region where the amplitude is directly proportional to tail current for a single resonance oscillator [30], the amplitude of differential oscillation (A) can be expressed as:

$$A \approx \frac{2}{\pi}\,\frac{I_{SS}}{G_d + G_t + G_s + G_{L,eff}}, \tag{3.11}$$

where I_{SS} is the dc tail current source, $G_{L,eff}$ models the effective differential conductance due to the series resistance of the inductors $G_{L,eff} \approx r\,C_{total}/(L \pm M)$, G_t conductance is mainly due to resistance series with tuning capacitance C_t ($G_t \approx Q_C\,C_t/\sqrt{C_{total}\,(L \pm M)}$) where Q_C is the effective quality factor of the tuning capacitor, and as mentioned before G_s and G_d are the differential conductance due to sensor and substrate/ active device, respectively. For a fixed amplitude (A_0) and control setting DC_0 as shown in Fig. 3.4(a), the ratio between I_{SS} and total conductance is fixed. Therefore, any variation in the conductance is translated to a variation in I_{SS} current determined by:

$$I_{SS0} - I_{SS1} \approx \frac{\pi}{2}\,A\,(\Delta G_s + \Delta G_{L,eff,1} + \Delta G_{d,1} + \Delta G_{t,1})\,. \tag{3.12}$$

The variation of I_{SS} does not depend only on ΔG_s but also on $\Delta G_{L,eff,1}$ ($\Delta G_{L,eff,1} \approx r\,\Delta C_s/\left(L \pm M\right)$), $\Delta G_{d,1}$ due to substrate loss variation with frequency and $\Delta G_{t,1}$. $\Delta G_{L,eff}$ and $\Delta G_{d,1}$ are comparable to ΔG_s and need to be calibrated using ΔC_s found from reading frequency. Another way to enhance the reading with less dependence on ΔC_s reading is to measure the difference in current in a different condition. In Fig. 3.4(b), digital control DC_2 is different form digital control DC_0 to achieve same frequency for both oscillators. The difference in current can be determined by:

$$I_{SS0} - I_{SS2} \approx \frac{\pi}{2}\, A\, \left(\Delta G_s + \Delta G_{t,2}\right). \tag{3.13}$$

Here, $\Delta G_{t,2}$ ($\Delta G_{t,2} \approx -Q_C\,\Delta C_t/\sqrt{C_{total}\left(L \pm M\right)}$) has less effect on the reading of ΔG_s and can be calibrated by a single time measurement of the oscillator in air. Therefore, $\varepsilon_r''\left(f_{MUT}\right)$ is determined by:

$$\varepsilon_r''\left(f_{MUT}\right) \approx \frac{G_{total,AIR}}{2\,\pi\, f_{MUT}\, C_{s0}} \left(\frac{I_{MUT} - I_{AIR}}{I_{AIR}}\right), \tag{3.14}$$

where I_{AIR} is I_{SS2} for air after $\Delta G_{t,2}$ calibration, I_{MUT} is I_{SS0} for MUT and $G_{total,AIR}$ is the total differential conductance of the oscillator in air ($G_{total,AIR} = G_t + G_d + G_{L,eff}$) . From (3.10) and (3.14), $\varepsilon_r'\left(f_{MUT}\right)$ and $\varepsilon_r''\left(f_{MUT}\right)$ are nearly linear functions with $(f_{AIR} - f_{MUT})$ and $(I_{MUT} - I_{AIR})$, respectively.

3.3 System Analysis

3.3.1 System Architecture

The proposed spectroscopy system is based on six LC-DCOs (a sensor and reference for three bands DCO_1, DCO_2 and DCO_3) to support the wide frequency range operation from 1 GHz to 6 GHz. The proposed block diagram is shown in Fig. 3.5(a), where there are two DCOs operating on different time intervals. Both

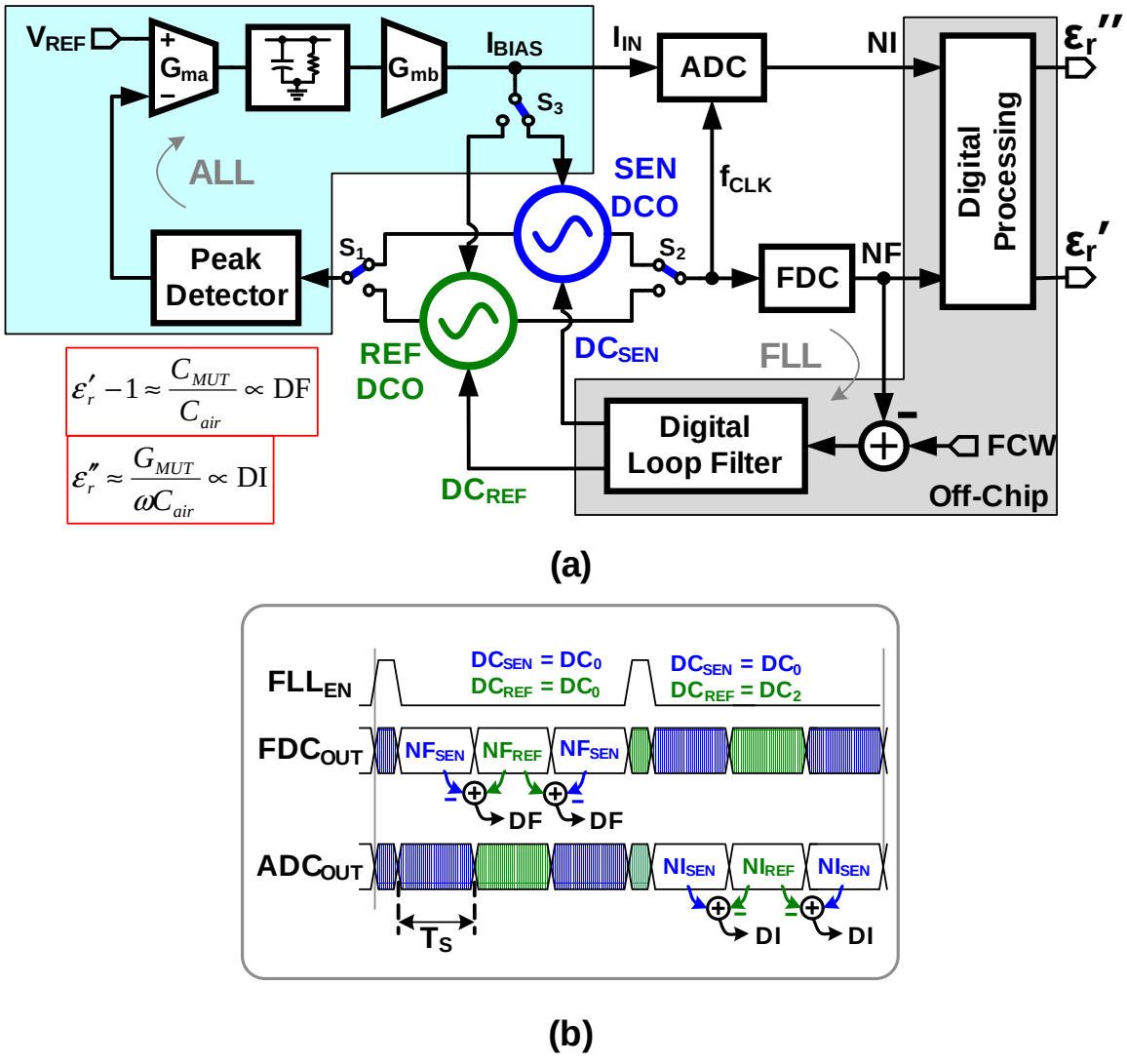


Figure 3.5: (a) Block diagram of the proposed sensor (the gray area is where the digital data is processed off-chip) (b) timing diagram showing CDS operation (CDS implementation is controlled by switches S_1, S_2 and S_3).

oscillators share the same control of the ALL to control the amplitude, while they have separate capacitor banks to change the frequency independently. Switches S_1, S_2 and S_3 are used such that only one oscillator is working at a time.

The proposed system consists of two loops: 1) an on-chip ALL loop which is used to lock the amplitude of the oscillation to A_0 ($A_0 \approx 1.4$Vpp deferentially), and

2) an off-chip frequency-locked loop (FLL) to adjust the digital controls DC_{SEN} and DC_{REF} controlling sensing and reference oscillators, respectively. The FLL is required to lock the sensing oscillator to f_{MUT} using the frequency controlled word (FCW). The output DC_{SEN} which is saved as DC_0 applied to both sensor and reference oscillators during ε'_r measurement. The FLL is enabled again to lock the reference oscillator to f_{MUT} with the output DC_{REF} is saved as DC_2. During, ε''_r measurement, $DC_{SEN} = DC_0$ and $DC_{REF} = DC_2$.

In Fig. 3.5(a), a 32-bit on-chip frequency-to-digital converter (FDC) is used to convert the frequency of its input clock to a digital word using a high-speed counter and a sampler with reading NF as a digital stream updated every sample time T_S ($T_S = 1/f_S$). Furthermore, the biasing current to the oscillators is mirrored and fed to an integrating analog-to-digital converter (ADC) with numeric output as NI updated every sample T_S time . The timing diagram is shown in Fig. 3.5(b), where the final readings are DF and DI proportional to $\varepsilon'_r(f_{MUT})$ and $\varepsilon''_r(f_{MUT})$, respectively. The outputs DF and DI are calculated using correlated double sampling (CDS) to minimize the effect of flicker noise and drifts.

3.3.2 Sensitivity and Correlated Double Sampling (CDS)

The sensitivity of the sensor is defined by the minimum detectable variation in ε'_r and ε''_r. The standard deviation (σ_f) of the frequency and the standard deviation of the current (σ_i) read by the counters can be calculated by the following equations [56]:

$$\sigma_f = \sqrt{\int_{f_{min}}^{\infty} S_f(f) \, \frac{sin^2(\pi f T_S)}{(\pi f T_S)^2} \, df}, \tag{3.15}$$

$$\sigma_i = \sqrt{\int_{f_{min}}^{\infty} S_i(f) \, \frac{sin^2(\pi f T_S)}{(\pi f T_S)^2} \, df}, \tag{3.16}$$

where $S_f(f)$ is the power spectral density of frequency fluctuations, $S_i(f)$ is the power spectral density of the DCO dc biasing current and f_{min} is the minimum frequency for integration which is the inverse of the observation interval (T_{obs}). LC-based open loop oscillators have low phase noise where they can achieve high sensitivity in measuring ε_r'.

The sensitivity of measuring the bias current of the oscillator is affected by all the elements that contribute to the circuit bias current and the reference current used in the current ADC. Since Flicker noise dominates the noise at low frequencies, σ_f and σ_i are determined by flicker $1/f$ noise behavior. Both σ_f and σ_i increase with T_{obs} due to the nature of flicker noise, therefore, T_{obs} should be limited and fixed for comparison. To enhance the sensitivity of the sensor, the impact of flicker noise has to be mitigated.

The most effective methods to minimize flicker noise are chopping and CDS. CDS is preferable in this system since it is inherently a sampled system. LC oscillators have different noise sources contributing to phase noise and amplitude noise. Phase noise is translated to an error in ε_r', while amplitude noise is translated to an error in ε_r''. The LC tank and the cross-coupled devices are replicated for each oscillator ($\mathrm{DCO_{SEN}}$ and $\mathrm{DCO_{REF}}$) and their noise cannot be canceled by CDS. Due to the difficulty of having a switch with very low resistance and small capacitance, a switch between the sensor with MUT and a sensor in the air was avoided. Using a technology with a smaller feature size, a direct switch at the sensor can be designed to minimize the flicker noise. In Fig. 3.5, CDS is designed to cancel all noise sources except the noise due to the core of the oscillators. The dominant source of flicker noise is the peak detector that senses the amplitude of oscillation since the size of the peak detector transistors should be small to avoid adding extra capacitance loading the oscillators.

Behavioral modeling of the oscillator can help to simulate the transfer function of noise sources with and without CDS, as shown in Fig. 3.6. The oscillator tank is modeled as a shunt R-C circuit, where the dc voltage on this shunt R-C represents the oscillator amplitude. The value of the shunt resistance can be modeled as $R_{shunt} = 1/\pi G$ to determine the single-ended amplitude at dc as $A = I_{bias}/\pi G$. C_{shunt} is adjusted to have bandwidth $f_{osc}/2Q$. Since the highest contributor of flicker noise in LC-DCOs is the AM-FM conversion of amplitude noise to phase noise, the model is based on finding the amplitude noise and use df/dA factor extracted from measurements, shown in Fig. 3.7, when ALL is off. An integrator with a sample and hold is used to model the change from frequency to phase where edges are counted. This model can predict the noise in the frequency reading accurately, while avoiding the high frequency oscillation to have faster simulation time. The ALL circuit is simulated using its transistor-level implementation since it does not have high frequency signals.

Noise sources that do not affect the amplitude at low frequencies are not modeled to have faster simulation time by not including the transitions at f_{osc}. Furthermore, their effect on phase noise at frequency shifts less than 1 kHz can be neglected. Noise sources n_{mb1} and n_{mb2} (modeling the noise of cross-coupled device and the biasing transistor of the DCO) do not affect the noise of the frequency since they are divided by the loop gain of the preceding lossy integrator. n_{ALL} (modeling input referred noise of ALL circuit) is the dominant noise source to affect the frequency reading where peak detector small devices cause higher flicker noise at peak detector input. Transient noise analysis is used for simulating 2,200 samples with a sample rate (f_S = 10 Hz) to validate the effect of CDS on frequency reading, as shown in Fig. 3.8. The frequency noise with CDS is nearly half of the frequency noise without CDS. Additionally, CDS has the ability to cancel any low frequency variations such

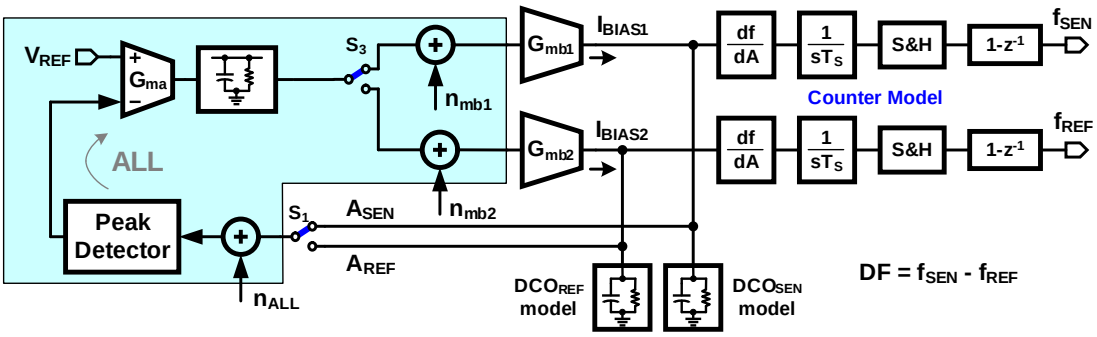


Figure 3.6: The model used to simulate the effect of CDS on frequency reading.

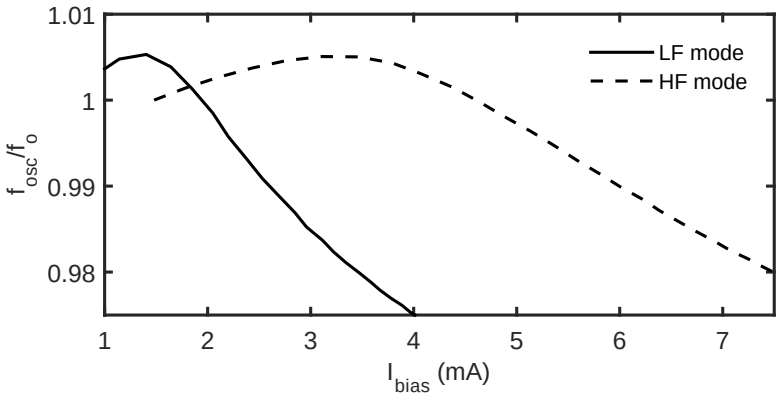


Figure 3.7: The measured relation between bias current and frequency shifts from f_o when ALL is off.

as temperature and humidity drifts. The simulated σ_f with CDS is about 0.28 ppm which is slightly lower than the measured σ_f ($\sim$ 2.1 ppm) due to the inaccuracy of flicker noise models and the estimated AM-FM df/dA conversion factor.

3.3.3 Selectivity of the Sensor

The selectivity of LC based sensors can be enhanced by minimizing the effect of ε_r'' on ε_r' reading, and vice-versa. From (3.3) frequency is independent on G_s to the first order, but the frequency is affected by ε'' as a secondary effect due to the

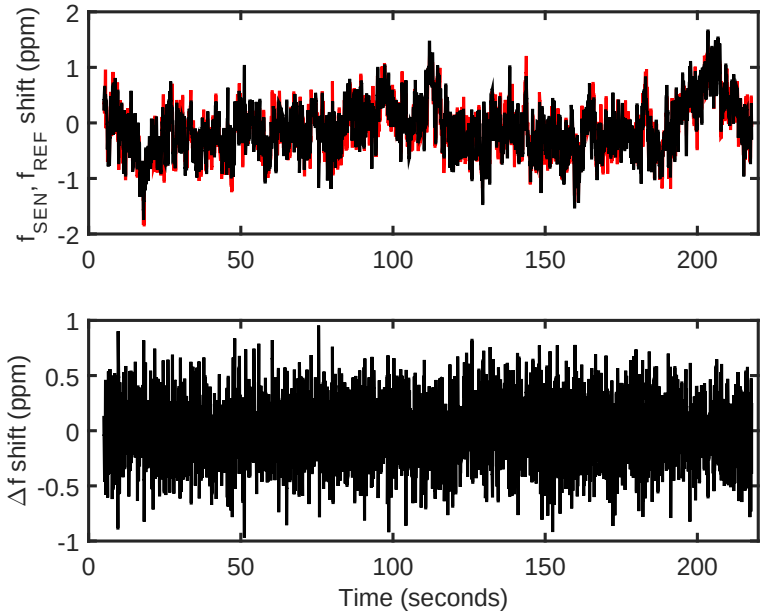


Figure 3.8: Transient noise simulation results show the effect of CDS on frequency reading.

variation of the oscillation frequency with oscillation amplitude. This phenomenon is called AM-FM conversion due to the variation of the average capacitance with amplitude [30]. To minimize this effect, the analog controlled varactors are replaced by digitally controlled varactors, and an ALL is used to fix the amplitude of both readings in air and with the material. Therefore, the reading of ε' is the frequency difference between an oscillator with MUT and another oscillator in air for the same control word and the same amplitude.

Minimizing the effect of ε'_r on ε''_r reading is challenging since the losses of the inductor and the tuning capacitor are functions of the frequency of oscillation which varies with ε'_r. To solve this issue, the tuning capacitance is used to compensate the effect of ε'_r on the frequency by providing fixed frequency for the oscillator with MUT and the oscillator in air. For compensating the effect of the change of the tuning

capacitor on loss, a lookup table is used to determine increased bias current due to changing tuning capacitor (ΔI_{corr}). This value should be added to the difference between the bias current of the oscillator with MUT and oscillator in air.

Another source of the interference between ε_r' and ε_r'' readings is the series resistance of the sensor. If the sensor has a series resistance (r_s) and assuming $r_s G_s << 1$, the admittance of the sensor (Y_s) can be calculated by:

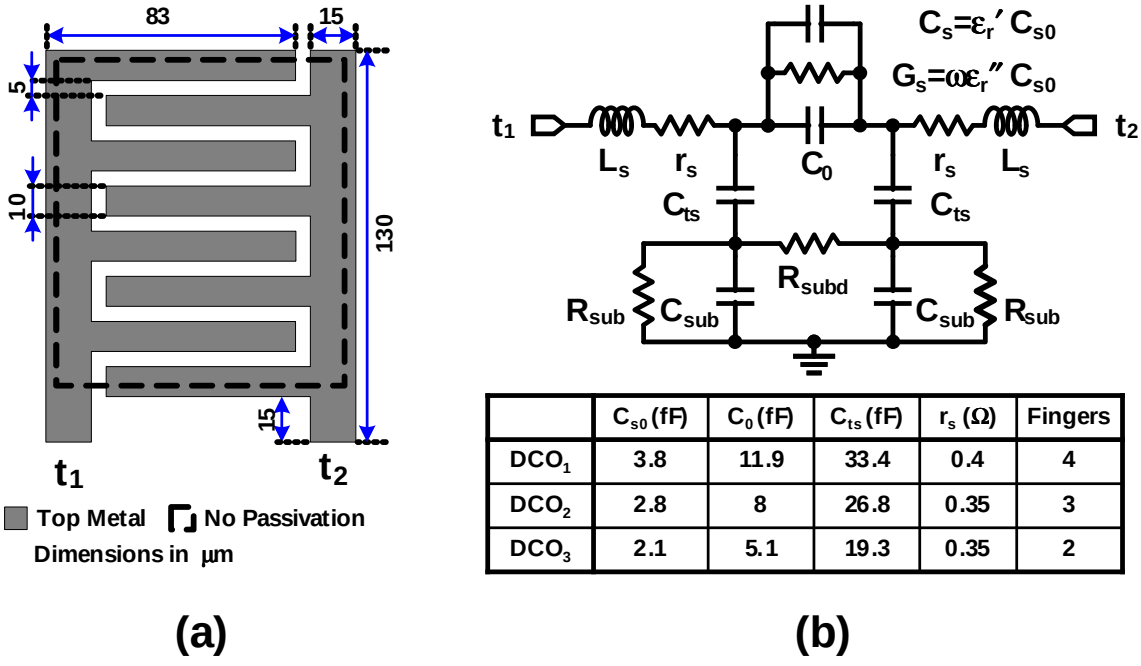
$$Y_s(\omega) = j\,\omega\,C_{eff} + G_{eff} \approx \frac{j\,\omega\,C_s + G_s}{1 + 2\,r_s\,G_s + r_s^2\omega^2 C_s^2}, \tag{3.17}$$

where G_{eff} is the effective conductance of the sensor with r_s, and C_{eff} is the effective capacitance of the sensor with r_s. The effect of r_s is to couple the reading of ε_r' and ε_r'' minimizing the selectivity of the reading. To preserve high selectivity of the sensor, r_s is chosen to be less than 0.5 Ω.

3.4 Circuit Implementation

3.4.1 Sensor Implementation

The capacitive sensor is centered in the chip to make the contact area with MUT away from the bondwires and pads. The sensor is an interdigitated capacitor, as shown in Fig. 3.9(a). The capacitor is implemented using the top metal where an opening in the passivation layer is used to have direct contact of the MUT. The technology used has six metal layers where the top-metal has 4 μm thickness and 9.94 μm separation from substrate (conductivity $\sim$ 7.4 S/m). The circuit model of the sensing capacitor based on electromagnetic (EM) simulation using Sonnet [29] is shown in in Fig. 3.9(b), where L_s ($\sim$ 40 pH) and r_s ($\sim$ 0.4 Ω) model the series inductance and resistance of the capacitor, respectively, C_0 models the direct interdigitated capacitance that is not affected by the MUT, C_{ts} models the capacitance to substrate, C_{sub} models the substrate capacitance, R_{sub} models the substrate resis-



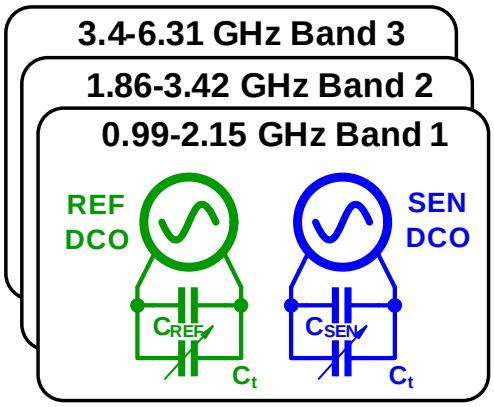
	C_{s0} (fF)	C_0 (fF)	C_{ts} (fF)	r_s (Ω)	Fingers
DCO_1	3.8	11.9	33.4	0.4	4
DCO_2	2.8	8	26.8	0.35	3
DCO_3	2.1	5.1	19.3	0.35	2

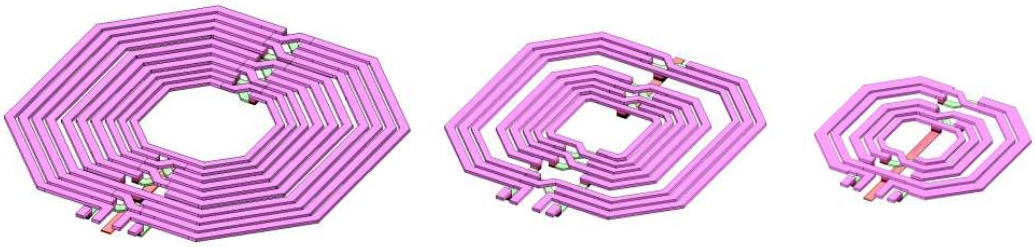
Figure 3.9: (a) Layout of the sensing capacitor in DCO_1, (b) model of the sensing capacitors with parameters for DCO_1(1-2.2 GHz), DCO_2 (1.9-3.4 GHz) and DCO_3(3.4-6.3 GHz)

tance, and R_{subd} models the differential substrate resistance. Since there are three different oscillators for the three different frequency ranges, there is a different sensing capacitor for each oscillator. The parameter of each sensing capacitor is shown in Fig. 3.9(b), where C_{s0} decreases for oscillators working at higher frequencies.

3.4.2 DCO Implementation

Two different oscillators are employed in the sensor architecture shown in Fig. 3.5(a): sensing DCO and reference DCO, where only one oscillator is operating at a time. For measuring ε_r' and ε_r'' at a certain frequency, there are different bands of operation. In each band, two oscillators were selected as the sensing DCO and reference DCO with similar transformers. DCO_1, DCO_2 and DCO_3 are used for Band 1 (0.99 to 2.15 GHz), Band 2 (1.86 to 3.42 GHz) and Band 3 (3.4 to 6.31 GHz), respectively.





DCO_1 Transformer DCO_2 Transformer DCO_3 Transformer

	L	k	n_1	n_2	$D_{1,outer}$	$D_{1,inner}$	$D_{2,outer}$	$D_{2,inner}$	C_{max}	C_{min}	$f_{min,L}$	$f_{max,L}$	$f_{min,H}$	$f_{max,H}$
DCO_1	9.3	0.396	4	6	400	296	284	136	1980	920	0.995	1.456	1.513	2.214
DCO_2	4.4	0.316	3	5	314	242	207	85	1216	710	1.886	2.468	2.616	3.424
DCO_3	1.35	0.336	2	3	227	170	150	73	1216	710	3.399	4.447	4.820	6.309
unit	nH				µm	µm	µm	µm	fF	fF	GHz	GHz	GHz	GHz

Figure 3.10: Diagram showing the operating bands of the three oscillators and the 3D of the transformer of each DCO where the table defines the parameters of the sensing DCO in air, and the frequency bands are defined using EM + post-layout simulations.

These frequency bands are determined using post layout and EM simulations. The 3D model of the transformers used in the DCOs are shown in Fig. 3.11 with their parameters extracted from EM simulations, where k is the mutual coupling factor of the transformer ($k = M/L$), $D_{1,outer}$ is the outer diameter of the outer inductor, $D_{1,inner}$ is the inner diameter of the outer inductor, $D_{2,outer}$ is the outer diameter of the inner inductor, and $D_{2,inner}$ is the inner diameter of the inner inductor. $C_{max}$and

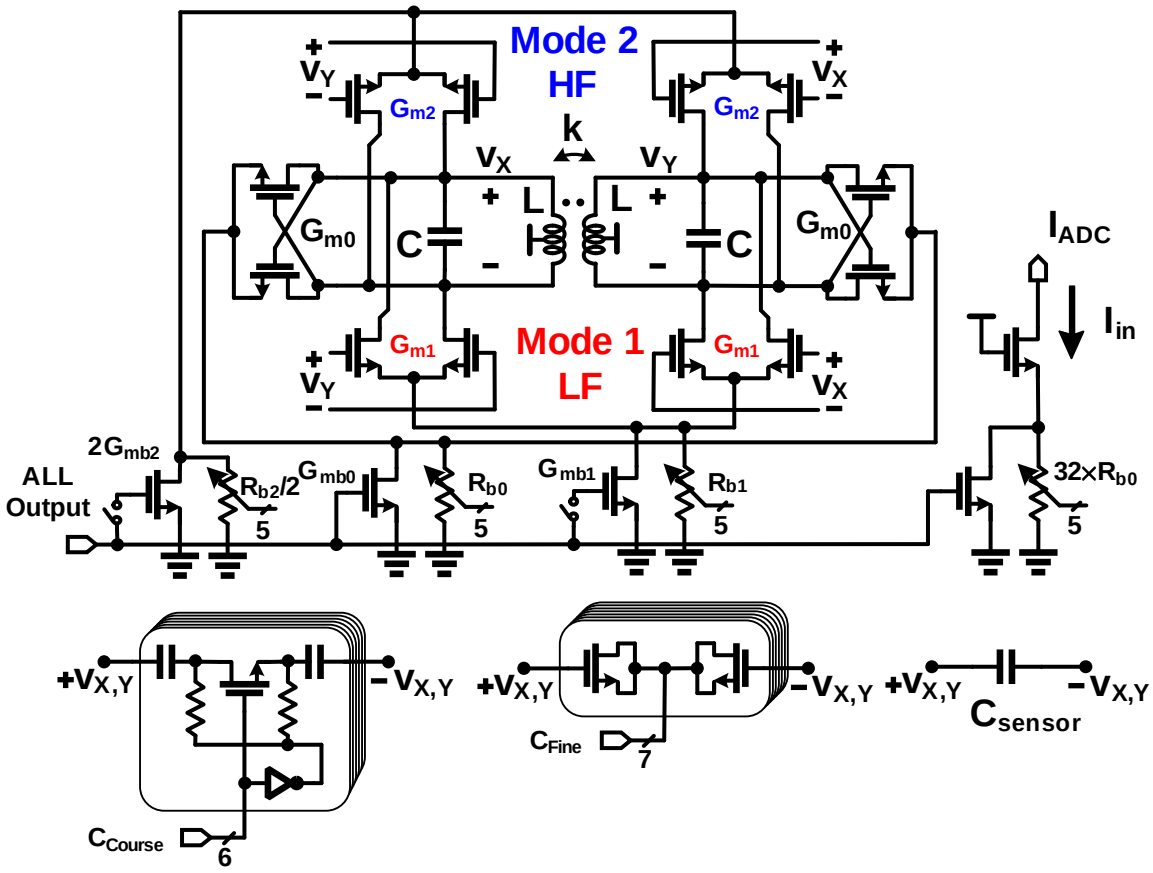


Figure 3.11: Schematic of a single DCO.

C_{min} are the maximum and minimum capacitances of sensing DCO in air, respectively. The values of L are adjusted for best quality factor (Q) for the transformer to enhance phase noise and minimize dc power consumption.

The capacitance tuning is implemented using two capacitor banks: 1) coarse capacitor bank (6 bits) implemented using metal-metal capacitors and series switches, 2) fine capacitor bank (7 bits) implemented using NMOS capacitors in inversion mode. Due to technology limitation, the frequency ranges at Bands 2 and 3 are less than Band 1, because of the smaller capacitor bank. Each oscillator is biased using a different tail current source to bias G_{m0}, G_{m1} and G_{m2} in Fig. 3.11. G_{m0}

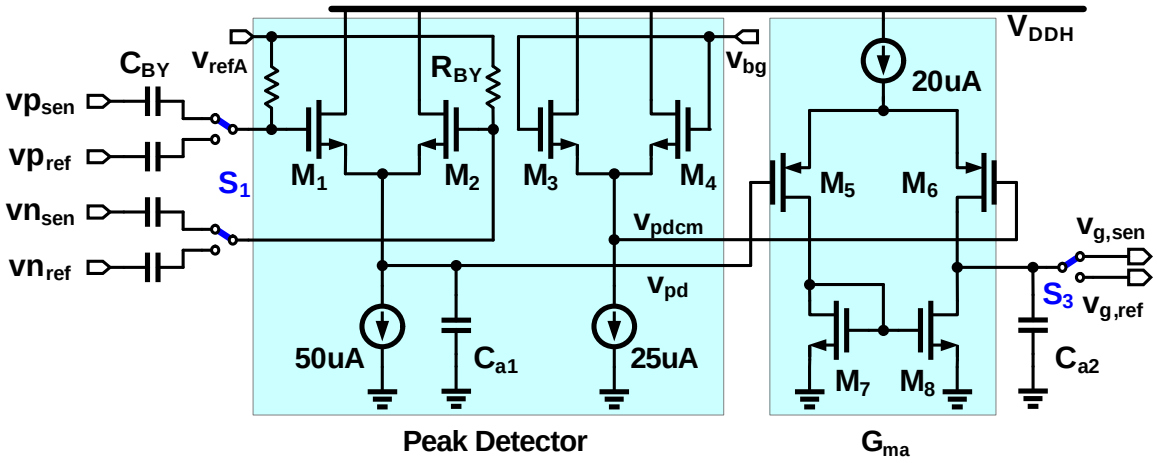


Figure 3.12: Schematic of the ALL where the amplitude is adjusted by the difference between v_{bg} and v_{refA}. Switches S_1 and S_3 control the ALL to activate DCO_{sen} or DCO_{ref}.

and G_{m1} have the same size and biasing current, while G_{m2} has double the size and biasing current for the increased loss in the higher frequency mode (3.9). The current consumption of the oscillator ranges from 2 mA to 13mA from 1V supply.

3.4.3 ALL Circuit

ALL circuit has mainly two functions: 1) stabilizing the frequency reading and minimizing the effect of ε_r'' on ε_r' reading, 2) locking the amplitude to preserve fixed relation between the biasing current and the measured conductance. Fig. 3.5 shows the schematic of the ALL circuit including three blocks: 1) CDS switches ($S_1$and S_3) to select sensing oscillator or reference oscillator, 2) peak detector block, 3) transconductor G_{ma} with capacitor C_{a2} to form an integrator. The peak detector block is a simple differential pair (M_1 and M_2) with gates connected to oscillator outputs, as shown in Fig. 3.12.

Since M_1 and M_2 devices are loading the oscillator, their sizes should be small. M_1 and M_2 pass current when the gate voltage is higher than the source. In this

case, capacitor C_{a1} is charged to the peak value of the gate minus the threshold voltage. To eliminate the effect of the process and temperature variations, a replica cell of the peak detector is used (M_3 and M_4) where the amplitude information is the difference between v_{pd} and v_{pdcm}. Since the amplitude is required to be compared to a value for feedback loop, the value is set implicitly using the dc voltage of the gates of the peak detector where the setting value should be the difference between v_{bg} ($\sim$ 850 mV) and v_{refA} ($\sim$ 690 mV). The ALL forces v_{pd} and v_{pdcm} to be equal ($\sim$ 390 mV) which is low enough to use PMOS transistors (M_5 and M_6) as G_{ma} inputs. The dominant pole of the ALL is determined by the output resistance of G_{ma} and C_{a2}($\sim$ 50 pF) acting as an integrator with zero gain at $G_{ma}/C_{a2} = \omega_{int}$ angular frequency. The loop stability is controlled by lowering G_{ma} such that the unity gain frequency is far less than the non-dominant poles with settling time of 2μs.

3.4.4 Frequency to Digital Converter (FDC) and Dividers

The FDC is a 32-bits synchronous frequency counter, shown in Fig. 3.13(a), where the input clock (f_{CLK}) triggers the two least significant bits (LSBs), $f_{CLK}/4$ triggers the following six bits and $f_{CLK}/256$ triggers the rest of the bits. The output of the 32-bits counter is sampled by f_S and saved in a 32-bits register. Since the maximum input frequency to the counter is limited by the technology to 1 GHz, the output frequency of the DCO needs to be divided to be in the operating range of the counter. Furthermore, the output of the DCO has to be converted from differential to CMOS level such that it can clock the CMOS counter. Since there are three oscillators with different frequency bands, dividers and buffers are designed for each band, as shown in Fig. 3.13(b). For band 1, a buffer is connected directly to the DCO_1 converting the differential signal to CMOS rail to rail single-ended output. The buffer has two inverters biased in their high gain point where the oscillator

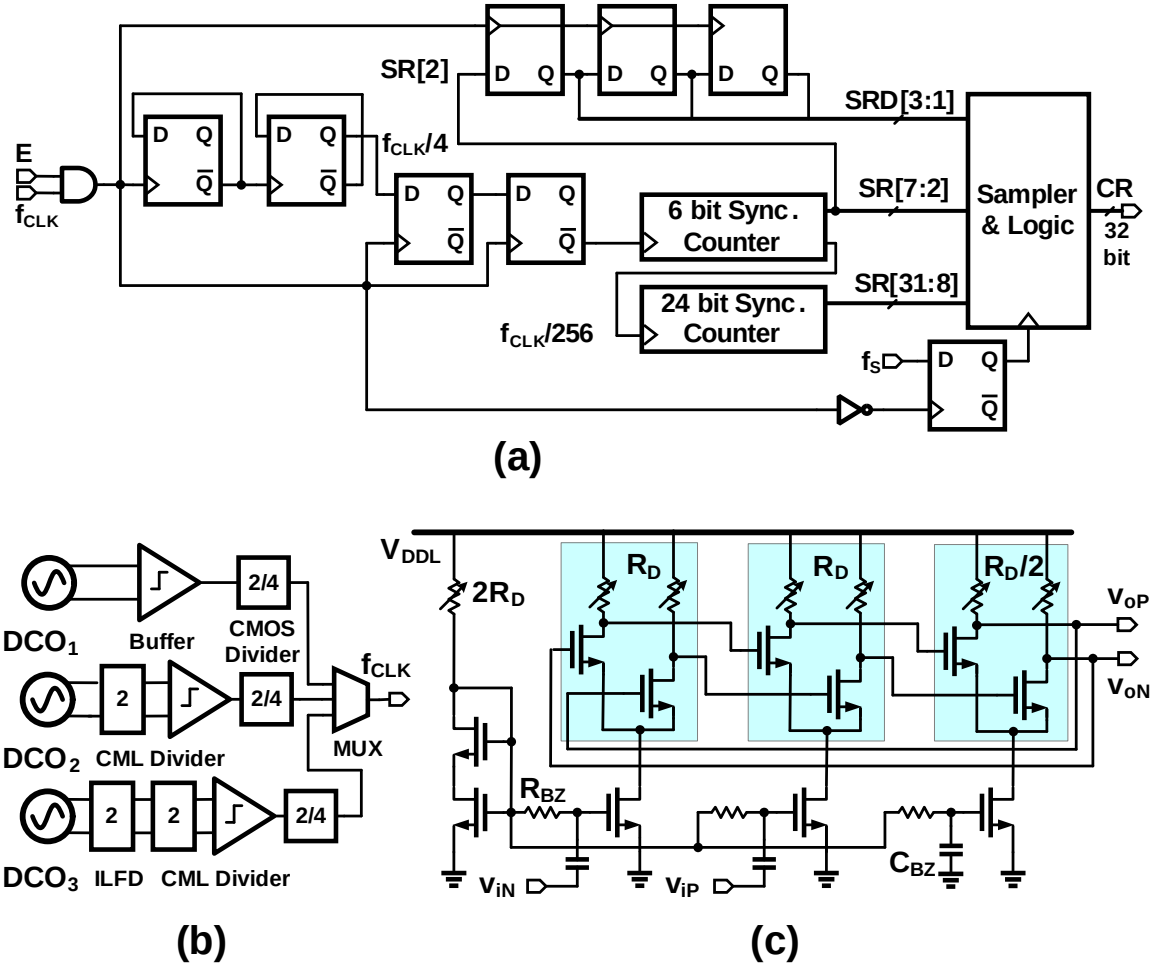


Figure 3.13: (a) Block diagram of the synchronous counter, (b) block diagram of dividers and buffers configurations for all bands, (c) schematic of ILFD for DCO_3 based on three stages ring-oscillator.

output is ac-coupled at the input of the inverters. The buffer is followed by a divider by 2 for the lower frequency range or by 4 for the higher frequency range. The measured power consumption of the buffer, the counters and the clock distribution is 5-6 mW from 1.65V supply.

For the second frequency band, the oscillator is followed by a current mode logic (CML) divider by two which is followed by a buffer same as the first frequency band.

The CML divider is directly connected to the oscillator with dc power consumption of 2.1 mW from 1 V dc supply. For the third band, DCO_3 is followed by an injection locking frequency divider (ILFD) to divide the frequency by 2 to lower the current consumption required by a divider at this high frequency for 0.18μm technology. The ILFD is a simple three stages differential ring oscillator with programmable load resistance R_D (2 bits), as shown in Fig. 3.13(c) [57]. Ring oscillators have small area and wide injection locking range. The power consumption of ILFD is configurable using R_D setting from 1.1 mW to 2.1 mW using 1 V dc supply. The input clock is injected deferentially to two stages using ac-coupling, while the third stage is connected to ground, where the ring oscillator is tuned to oscillate at half the input frequency.

3.4.5 Current Integrating ADC

The current ADC has to be linear and low noise with a low power consumption. Since the speed is not critical for the ADC, integrating ADC was the most appropriate topology. The current is compared to a reference current I_{ref} ($\sim$ 200 μA) and converted to a pulse width modulated (PWM) signal where the width of the pulse is proportional to I_{in}/I_{ref}. The sampling rate of the PWM signal T_{OUT} is controlled by an external clock (f_{si} $\sim$ 8-10 MHz). The schematic of the integrating ADC is shown in Fig. 3.15. Signals S_{N1} and S_{N2} are used to control the NMOS switches that discharge capacitors C_A using input current I_{in} (current drawn by the DCO current mirror shown in Fig. 3.11), while S_{P1} and S_{P2} are used to control the PMOS switches that charge capacitors C_A using reference current . Since $I_{in} \leq I_{ref}$, the charging time is less than the discharging time and $T_{charging} = I_{in}/I_{ref} \times T_{si}$ where $T_{si} = 1/f_{si}$. The control signals are generated from v_M and v_N signals, where their voltage levels are compared to v_{HIGH} and v_{LOW} voltage levels using four comparators, as shown

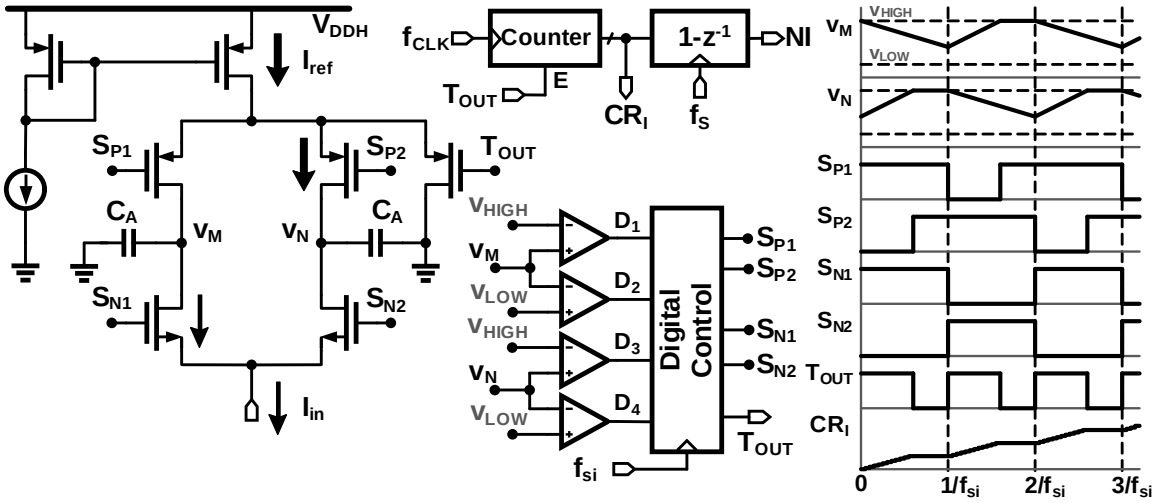


Figure 3.14: Schematic of the integrating ADC to convert current to PWM signal (T_{OUT}) with sampling frequency f_{si} which controls the enable of a counter with sampling frequency f_S.

in Fig. 3.15. The output signal T_{OUT} controls a counter with clock f_{CLK} (same one used for measuring frequency), such that the pulse width modulated signal is filtered and converted to the digital counter reading CR_I. NI is the difference between two consecutive CR_I readings, where $I_{in} = NI/NF \times I_{ref}$. The total dc power consumption of the ADC is 670 μW without including the counter. The measured ADC output can be compared to the measured current of the oscillator for maximum R_b setting (~ 31) in Fig. 3.11, as shown in Fig. 3.15. The results show good linearity with a gain difference between HF mode and LF mode. This difference is not critical since each reading is calibrated at the same frequency and the same mode.

3.5 Measurement Results

The chip is fabricated using 0.18 μm IBM CMOS process with dual supplies (1 Vdc and 1.65 Vdc). The low supply voltage is used for the DCOs, ILFD and CML divider. The high supply voltage is used for the digital circuits, the buffers,

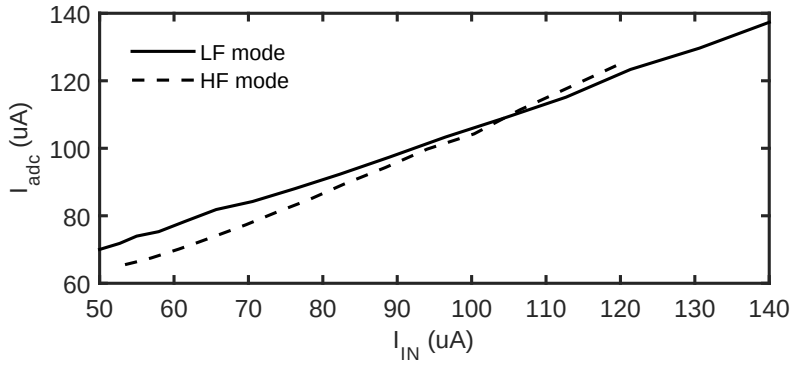


Figure 3.15: Measured ADC reading versus input current estimated from the dc current of the oscillator for DCO_1 at R_b setting equals 31.

ALL circuit and the integration ADC. The dc power consumption depends on the frequency and mode of operation (3.5-17 mW) from 1 V dc supply and (4-6 mW) from 1.65 V dc supply. The die photograph is shown in Fig. 3.16. The chip area is 2.4 $\times$ 2.6 mm^2 where the dominant area is the area of the transformers and the capacitance bank of the oscillators. The sensing capacitors from each band are located close to each other to localize the sensing area. The chip is tested using the PCB in Fig. 3.17.

3.5.1 Electrical Characterization

3.5.1.1 Phase Noise and Frequency Range

The frequency ranges of the oscillators are determined by the three oscillating bands where each band is divided to lower sub-band and higher sub-band. The phase noise of the oscillator at 1GHz is measured by spectrum analyzer E4446A, where f_{CLK} is buffered and measured. The phase noise of DCO_1 at minimum frequency after division by 2 setting ($\sim$ 488 MHz) is measured with ALL "on" and "off", as shown in Fig. 3.18. When ALL is on, the phase noise at 1 MHz and 100 kHz offsets increases due to the added noise of the ALL loop, but the stability of the oscillation frequency is better as seen at the low-frequency offsets ($<$ 10 kHz).

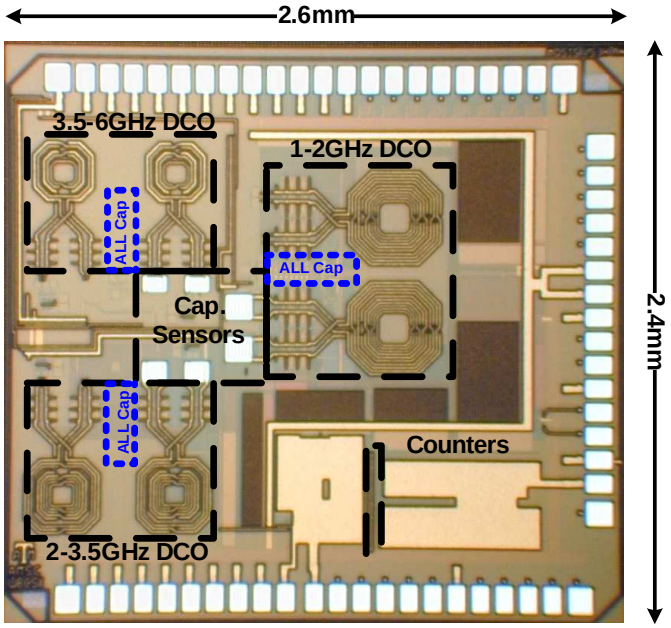


Figure 3.16: Die Photograph.

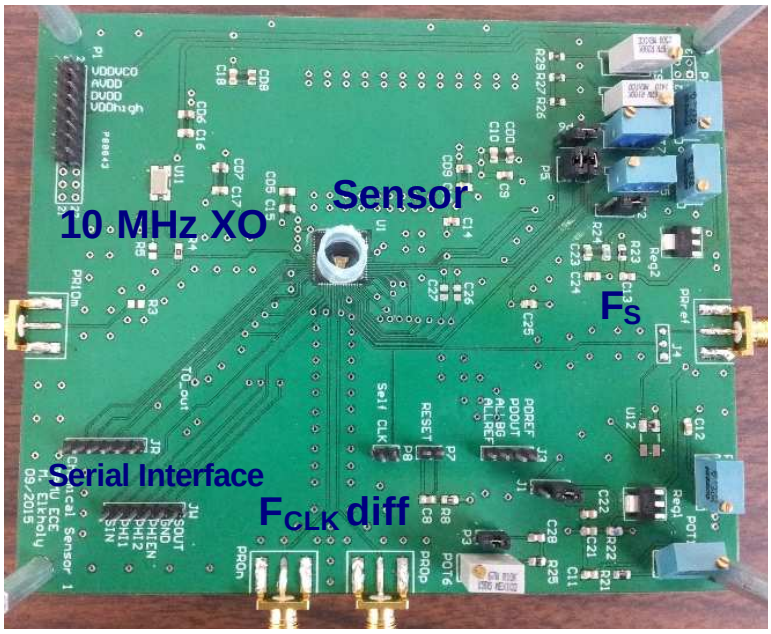


Figure 3.17: PCB used for testing the chip.

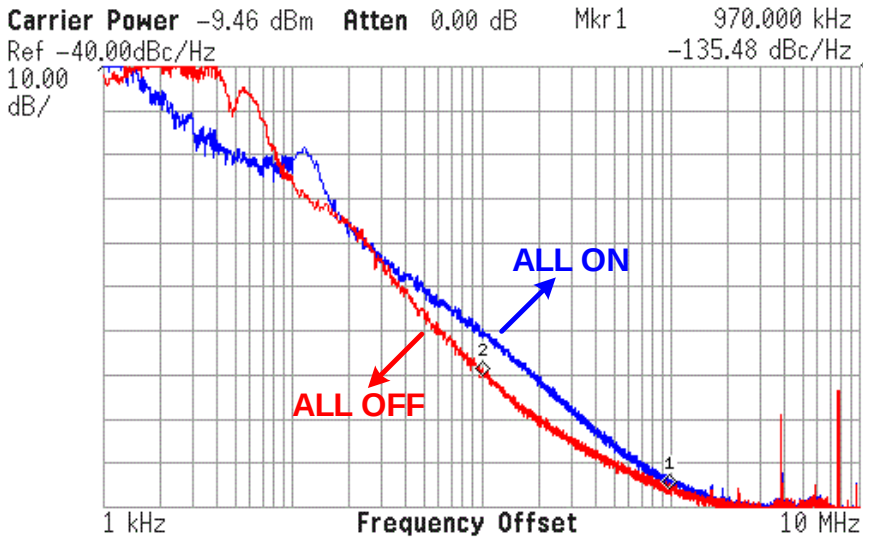


Figure 3.18: Phase noise at 488 MHz from lower band of DCO_1 after division by 2, where the blue curve is for ALL "on", while the red curve if for ALL "off".

In Fig. 3.19, the oscillator current versus frequency is plotted on a logarithmic scale in frequency to emphasize the comparison among the three bands. The frequency range has gaps between the lower sub-band and the higher sub-bands in each band due to higher unexpected values of the transformer coupling factor (k). The gaps can be avoided by lowering k and using smaller feature size technology to maximize the tuning range of the capacitance. The measured frequency gaps are from 1.417-1.53 GHz, 2.543-2.693 GHz, and 4.327-4.684 GHz. The frequency gaps will not affect the shape of the spectrum, since the variations of $\varepsilon_r'(f)$ and $\varepsilon_r''(f)$ are smooth relative to these frequency gaps.

The oscillator current of the higher sub-band is nearly double that of the lower sub-band due to the series resistance of the inductors (3.9). The phase noise at 1 MHz and 100 kHz offset frequencies are shown in Fig. 3.20 where the figure of merit (FOM) of the oscillators is between 182 dB to 172 dB at 1 MHz offset frequency while ALL is "on",

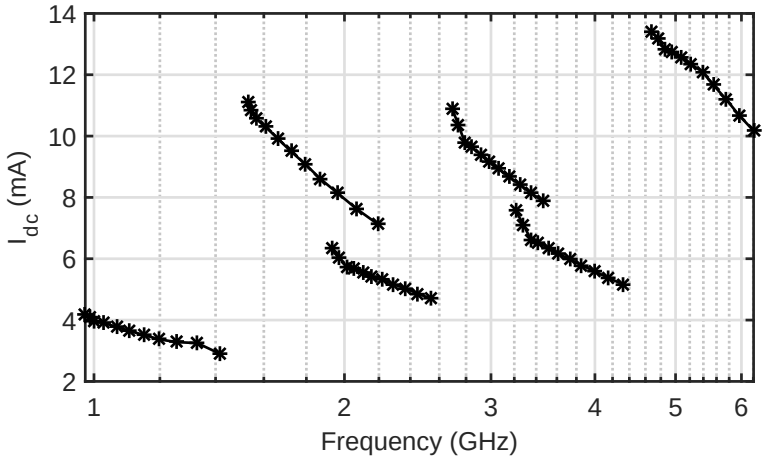


Figure 3.19: Current consumption versus frequency for the three bands with ALL "on".

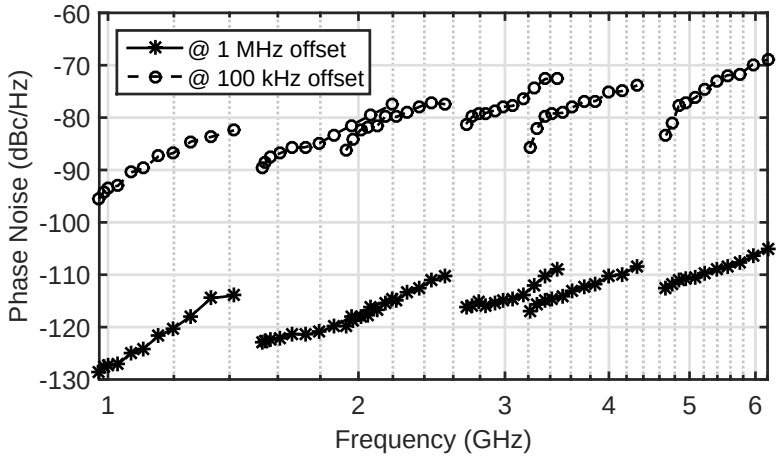


Figure 3.20: Phase noise at 1 MHz and 100 kHz offset frequencies for the three bands with ALL "on".

3.5.1.2 Noise Performance

Since the repeatability of the reading is critical, the frequency reading noise with a large number of samples is measured. The frequency shift noise is expected to be relatively low due to the low phase noise performance of LC-oscillators [1, 51].

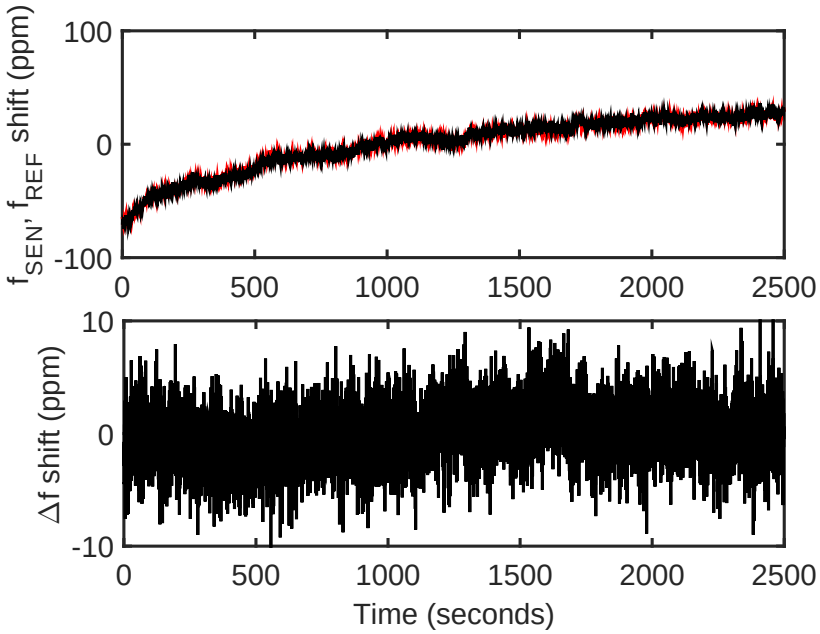


Figure 3.21: Frequency shifts of DCO_{SEN}, DCO_{REF} and the difference reading using CDS in ppm. (f_{CLK} = 515 MHz)

The counters' readings are sampled by a 4 Hz (T_S = 0.25 s) clock limited by the serial interface speed and they are monitored for 10,000 samples or 41.67 minutes. For DCO_{SEN} and DCO_{REF} running at 2.06 GHz and counter clock f_{CLK} of 515 MHz (division = 4), the shift of the frequency with time is shown in ppm (relative to 515 MHz) in Fig. 3.21. The standard deviation of Δf is 2.1 ppm after using CDS. CDS helps to cancel the common-mode flicker noise and the drift of the frequency with time or temperature variations. This variation means the standard deviation in capacitance reading is 3.6 aF.

Current variations are nearly two order of magnitude higher than frequency variations due to the low dependence of the frequency on bias current in LC-oscillators. The current variation of i_{SEN} and i_{REF} for 5,000 samples at 2 Hz (T_S = 0.5 s) is shown versus time in Fig. 3.21. The standard deviation of Δi is 110 ppm with CDS.

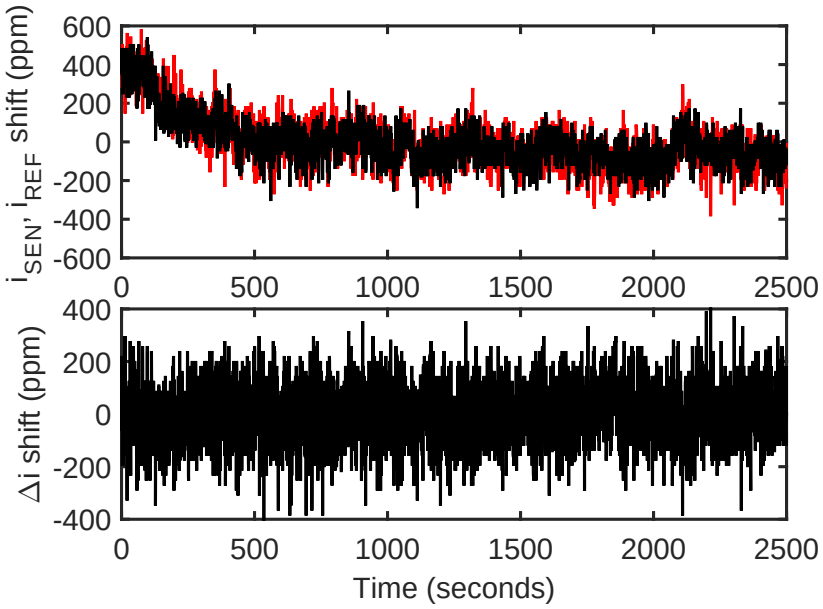


Figure 3.22: Current shifts of DCO_{SEN}, DCO_{REF} and the difference reading using CDS in percentage.

Due to this higher noise in measuring current, the error in measuring ε_r'' is expected to be much higher than the error measuring ε_r'. This represents the impact of the circuit noise. Another source of perturbations is the dependence of the material on temperature fluctuations. Therefore, 10 samples are acquired for each measurement to enhance the accuracy.

3.5.2 Measurement Using Ethanol-Water Mixture

For measurements of the chemicals, 10 samples are acquired at each frequency and averaged to enhance accuracy. Ethanol-water mixtures are measured to determine the capability of the sensor to measure the complex permittivity versus frequency. In Fig. 3.23, ε_r' was measured for ethanol-water mixtures between ethanol 100% to ethanol 60%. Ethanol 95%, ethanol 75% and ethanol 60% are used for quadratic calibration of the relation between frequency shifts and ε_r' [1]. The error in measure-

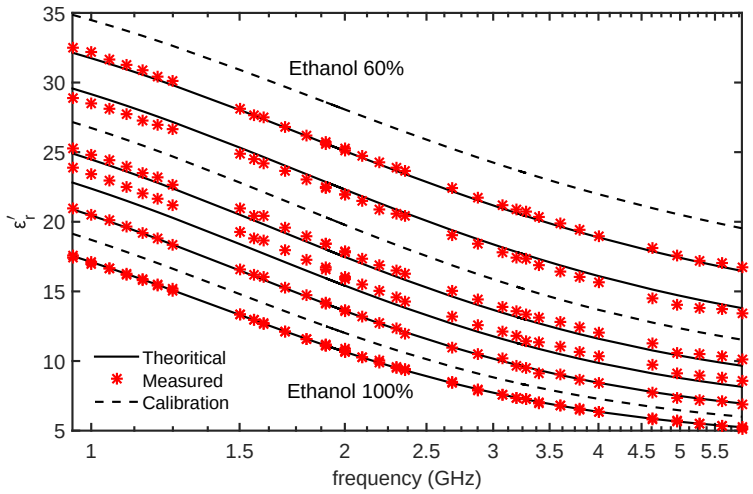


Figure 3.23: ε' measurement versus frequency for ethanol mixtures between 100% to 60% with step 5%, where calibration points are ethanol 95%, ethanol 75% and ethanol 60%.

ments is less than 2% except for ethanol 85% which may be due to the accuracy of preparation of the mixture. ε_r'' is measured for two ethanol-water mixtures: ethanol 85% and ethanol 70%, as shown in Fig. 3.24 (a) and (b) respectively. Air, ethanol 95% and ethanol 60% are used for quadratic calibration to relate dc current shifts to ε_r''. The worst case error is less than 5%, where the main sources of error are the high noise in current reading and inaccurate calibrations of the capacitor bank loss. The capacitor bank fine tuning causes higher losses than expected. At highest frequency band, the ALL loop fails to lock affecting the accuracy of reading of ε_r''.

3.5.3 Measurement Using PBS

Phosphate-buffered saline (PBS) characterization is critical to determine the conductivity of the medium used for preserving cells. The current shift readings can be used to determine the conductivity of PBS solutions with different concentrations ranging from 0.1X PBS to 1X PBS. Since PBS has the same profile of ε_r' similar

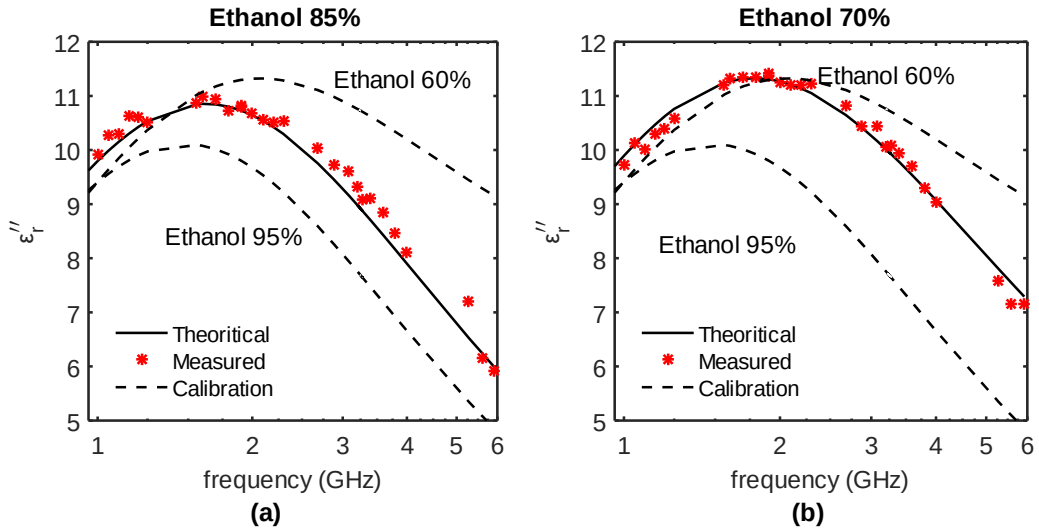


Figure 3.24: ε_r'' measurement versus frequency for (a) ethanol 85% mixture and (b) ethanol 70% , where calibration points are air, ethanol 95% and ethanol 60%.

to de-ionized (DI) water, all concentrations have the same frequency shifts. Different PBS solutions with different concentrations are measured versus frequency and their conductivity measurements are used to extract the value of PBS concentration of each solution using DI water and PBS 1X as calibrating mediums, as depicted in Fig. 3.25. The PBS 1X (from Thermo Fisher Scientific) with dc conductivity $\sigma_{PBS,1X} \sim 1.59 \pm 0.19$ S/m is diluted to different concentrations and the measured current shifts are used to determine the concentration of the PBS solutions with DI water and PBS 1X as calibration points. The error increases at higher frequency bands mainly due to two reasons: 1) the relative difference in total conductivity between PBS 1X and DI water decreases at higher frequencies since DI water ε_r'' increases at higher frequencies, 2) the accuracy of the ALL degrades at higher frequencies. To verify the variation of the measured total conductivity ($\sigma_t = \sigma + \omega\,\varepsilon_r''$, where σ is the conductivity of material) of PBS 1X with frequency, air, ethanol 95% and DI water are used for calibration to find the total conductivity of PBS 1X, as

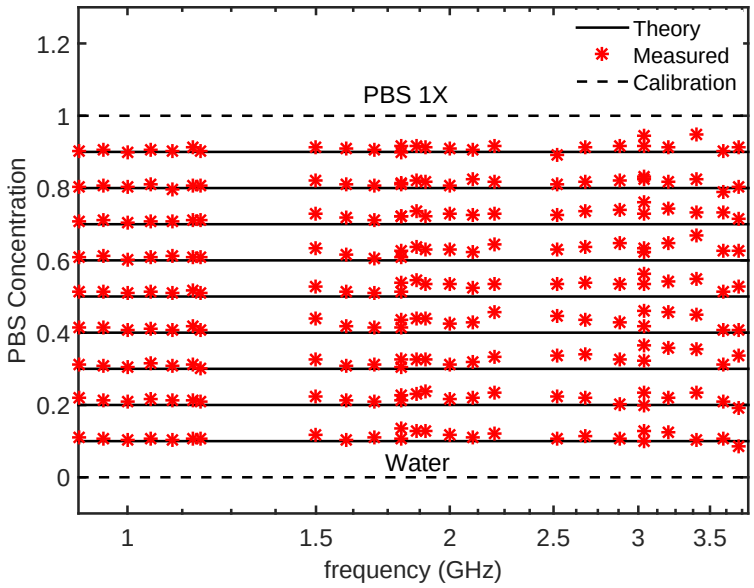


Figure 3.25: Concentration measurement of PBS solutions versus frequency using DI water and PBS 1X for calibration.

shown in Fig. 3.26.

The measurements results show comparable performance to wide-band spectroscopy systems [16, 17, 20] while achieving much lower power consumption. Furthermore, the sensitivity in measuring ε_r' in air (based on the standard deviation of Δf measurements) has comparable accuracy to systems of high accuracy in measuring ε_r' only at single frequency [18, 59]. The comparison between the spectroscopy system with recent literature is shown in Table 3.1. The system can measure complex permittivity using LC-oscillator with wider frequency range compared to [1], where CDS is implemented to enhance the sensitivity and stability of sensor reading with comparable power consumption. The sensor can work at high frequencies with lower power consumption compared to [16, 17, 20].

Table 3.1: Performance Summary and Comparison with State-of-The-Art BDS Systems

	This Work	Helmy [1] JSSC'12	Bajestan [16] MTT'14	Bakhshiani [50] JSSC'14	Elhadidy [20] MTT'14	Bakhshiani [17] TBCAS'15	Chien [58] IMS'13
Technology	0.18μm CMOS	90 nm CMOS	0.18μm CMOS	0.35μm CMOS	0.18μm CMOS	0.35μm CMOS	65 nm CMOS
Methodology	LC-Osc. freq. & current shift	LC-Osc. freq. shift & PLL	Excitation amp./phase	Excitation amp./phase	Ring Osc. freq. shift & PLL	Excitation amp./phase	Excitation amp./phase
Self Sustainability	Yes	Yes	No	No	Yes	Yes	No
Sensor Type	On-chip 2D Capacitor	On-chip 2D Capacitor	On-chip 2D Capacitor	Off-chip T. Line	On-chip 2D Capacitor	Off-chip 3D Capacitor	On-chip T. Line
Freq. Range [GHz]	0.98 - 6†	7 - 9	0.62 - 10	0.01 - 3	0.7 - 6	0.009 - 2.4	1-50
Permittivity Type	ε'_r , ε''_r	ε'_r only	ε'_r , ε''_r	ε'_r only	ε'_r , ε''_r	ε'_r , ε''_r	ε'_r , ε''_r
CDS Implemented	Yes	No	No	No	No	No	Yes
Osc. PN [dBc/Hz] (@ 1 MHz offset)	-128.3 dBc/Hz @ 1 GHz	-109.9 dBc/Hz @ 8.1 GHz	NA	NA	-75 dBc/Hz @ 3.3 GHz	-107 dBc/Hz @ 2.432 GHz	NA
Permittivity Error	Max 2% (ε'_r) (1- 6 GHz) Max 5% (ε''_r) (1- 3.8 GHz)	Max 3.7% (ε'_r)	RMS 1% (ε'_r and ε''_r)	RMS 6.4% (ε'_r) (0.5 - 2.5 GHz)	Max 3.7% (ε'_r and ε''_r)	RMS 0.7% (ε'_r) RMS 1.5% (ε''_r) (0.5 - 2.4 GHz)	$\sigma\left(\Delta\varepsilon_r/\varepsilon_r\right) \approx 1\%$ @ $\lvert\varepsilon_r\rvert = 4.45$ & 20 GHz
Freq. Noise [ppm]	RMS 2.1	RMS 222*	NA	NA	RMS 800	NA	NA
Power [mW]	10 - 24	16.5	65 - 72**	4 - 9**	69 - 140	61 - 94	114**
Die Area [mm^2]	6.24	6.25	9	9	6.25	10.89	1.2

* Calculated from the paper based on Δf(min) = 2 MHz at 9 GHz,
** Not including the dc power of the excitation source,
†The range has frequency gaps due to the multiple bands operation.

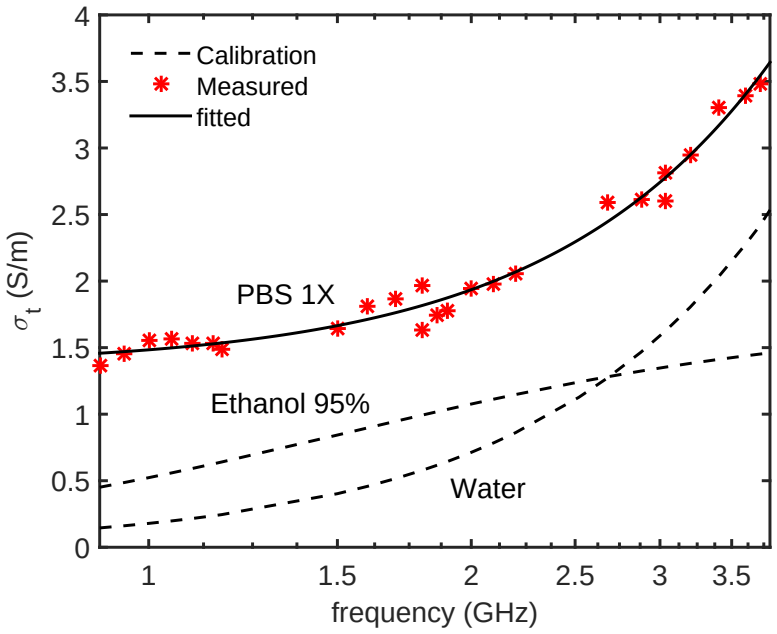


Figure 3.26: Total conductivity measurement of PBS 1X versus frequency using air, ethanol 95% and water for calibration.

3.6 Conclusion

A spectroscopy system is proposed using LC-based oscillator capacitive sensing. The sensor can measure the complex permittivity of different materials including de-ionized water and PBS at multiple frequencies in the 1-6 GHz range. The system has a reference oscillator to alleviate the effects of the temperature and drifts using a correlated double sampling (CDS) technique with 2.1 ppm random noise in frequency shift reading and 110 ppm in current shift reading. The sensor was tested with ethanol-water mixtures with different concentrations and achieved a maximum error of 2% in real permittivity and 5% in imaginary permittivity in 1-3.8 GHz frequency range.

4. LOW LOSS INTEGRATED CMOS ELECTRICAL BALANCE DUPLEXERS

4.1 Introduction

The pursuit of higher data rate in wireless communications will continue in the future to meet the ever increasing demands. The 3rd Generation Partnership Project (3GPP) standard has increased the number of frequency bands [60], where the multi-band operation is an essential requirement for all commercial cellular handsets. A frequency division duplexing (FDD) scheme is commonly used in 3G and 4G-FDD cellular handsets, such that the transmitter (TX) and the receiver (RX) are working simultaneously but in different frequency bands. The necessity to share the antenna between TX and RX urges the need for a duplexer to isolate between the transmit and receive paths. Conventionally, a surface acoustic wave (SAW) duplexer is used, because of its high isolation. With the increased number of bands, the RF front end complexity scaled significantly as shown in Fig. 4.1(a). Each band has a dedicated tuned SAW duplexer, **a** power amplifier (PA), and **a** low noise amplifier (LNA). As the number of supported bands increases, the cost of the tuned SAW duplexers can surpass the transceiver IC cost. Furthermore, the significant area allocated for the multiple SAW duplexers can limit the form factor of the cellular handset.

Different approaches have been demonstrated to address the aforementioned challenges. The first approach replaces SAW duplexers with bulk acoustic wave (BAW) duplexers [61, 62], because of their smaller size and lower temperature sensitivity.

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*© 2014 IEEE. Parts of sections are reprinted, with permission, from M. Elkholy, M. Mikhemar, H. Darabi and K. Entesari, "A 1.6-2.2GHz 23dBm low loss integrated CMOS duplexer", Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, San Jose, CA, 2014, pp. 1-4.

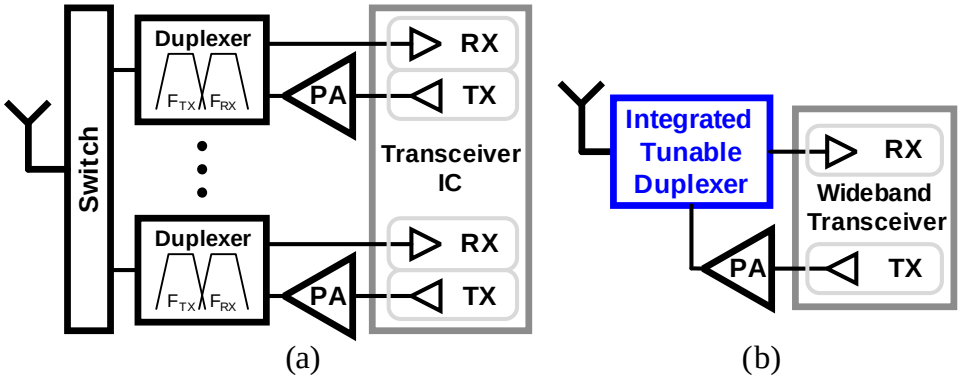


Figure 4.1: (a) Conventional FDD solution using multiple SAW duplexers , (b) Integrated FDD solution using tunable on-chip duplexer.

However, BAW duplexers are more expensive than SAW duplexers, so this approach does not resolve the cost challenge, even though the BAW cost is expected to decrease in the future by the advancements in BAW technology. A second approach relies on dual-band duplexers by combining two duplexers into a one to cut cost and area by a factor of two [63, 64]. However, the increased insertion loss of dual-band duplexers limits the performance.

A completely different approach relies on a tunable integrated duplexer with a wideband RX and a wideband PA**,** as shown in Fig. 4.1(b). This approach is considered optimal in terms of flexibility, cost, and area**,** but its implementation is very challenging. In the last decade, there were significant research efforts to develop a wideband SAW-less RX with a low noise figure (NF) and a high linearity performance as demonstrated in [65, 66]. A multi-mode multi-band PA with a highly promising performance is demonstrated in [67]. However, designing a wideband tunable duplexer with acceptable performance is an extreme challenge and is considered the bottleneck of this wideband approach.

A tunable duplexer can be implemented as a tunable lumped LC or a microstrip

filter [68–70], but the TX-RX isolation is usually limited (∼20dB). The performance of the duplexer is usually improved as the TX-RX frequency separation is increased, for example, UMTS-FDD band I. Furthermore, a cancellation circuit can be used to enhance the total isolation in a receiver architecture with TX leakage suppression as presented in [71, 72]. A wideband or a tunable circulator can also be used to provide about 20dB basic isolation, in conjunction with a TX cancellation circuit to cancel the residual TX signal at the LNA input [73, 74]. This approach usually has a low insertion loss that improves the total efficiency of the PA. However, the impedance mismatches at the antenna is considered a major drawback of this approach. The tunable duplexers mentioned above are not fully integrated, since LC filtering needs very high quality factor off-chip inductors, while circulators are bulky especially for wideband operation and cannot be integrated.

A fully integrated duplexer was first reported in [75]. It is based on an *electrical balance* between two paths in order to cancel the TX signal at the RX input. The electrical balance duplexer (EBD) relies on a hybrid auto-transformer to separate between TX and RX signals. An enhanced version was proposed later in [76] to enable a wider bandwidth operation, while achieving high isolation close to SAW duplexers. However, it could not support high power operation, because the PA signal appears as common-mode at the input of a differential LNA, degrading its linearity performance. To support higher TX power levels, a fully differential EBD was proposed in [77, 78]. Nevertheless, the drawback of this differential solution is the added balun at the antenna port which considerably increases the insertion loss of the duplexer.

This chapter presents a fully integrated tunable duplexer with a single-ended LNA that can handle high power operation up to 22 dBm. It is based on a cross-connected transformer topology without the need of any extra balun at the antenna.

The operation of the duplexer is verified by a prototype fabricated using a 0.18μm CMOS technology [79]. The rest of the chapter is organized as follows: Section 4.2 provides an overview of electrical balance duplexers (EBDs). Section 4.3 presents the proposed EBD architecture followed by a comprehensive analysis of its insertion loss and noise performance. Section 4.4 discusses the implementation details of the prototype EBD, while the measurement results of the prototype are shown in section 4.5. Finally, the key contributions of this work are summarized in section 4.6.

4.2 Passive Integrated EBDs

4.2.1 Reciprocity Concept

The main functionality of a duplexer is to deliver the TX power from the power amplifier (PA) to the antenna (ANT) and to deliver the RX power from the ANT to the low noise amplifier (LNA) at the same time. For a 3-port passive matched duplexer, the duplexer S-matrix can be described by:

$$S_{3p,ideal} = \begin{bmatrix} 0 & 1\,e^{-j\theta} & 0 \\ 0 & 0 & 1\,e^{-j\gamma} \\ 1\,e^{-j\theta} & 0 & 0 \end{bmatrix} \tag{4.1}$$

where ANT is port 1, TX is port 2 and RX is port 3, θ, γ and ϕ and are the phase shifts due to the delays in the different paths of the duplexer. In this case, the S-matrix is non-reciprocal, since the S-matrix for reciprocal materials should have elements $S_{nm} = S_{mn}$ (m$\neq$n) [80]. On the other hand, all passive integrated elements such as resistors, capacitors and inductors are reciprocal by nature, since they are made of isotropic materials. The ideal duplexer can be built using ferrite materials which have different permeabilities depending on the direction of propagation. This property is used to build circulators to circulate the RF power as seen in Fig. 4.2(a).

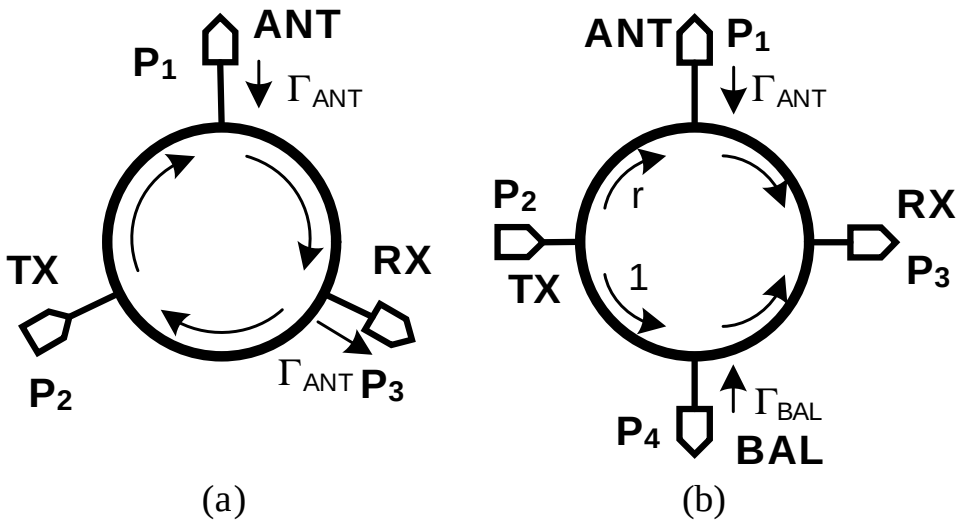


Figure 4.2: RF duplexer using (a) a circulator, and (b) an electrical balance.

Circulators are extensively used in base stations, but they are bulky and require strong magnetic fields. Furthermore, circulators usually have narrow bandwidth [81]. In practice, circulators cannot achieve very high isolation between the TX and RX signals, since any reflection at the ANT port will be considered as received signal from the antenna. Thus, the isolation is simply the return loss (RL) at the ANT port of the circulator.

Since a lossless passive wideband on-chip 3-port duplexer cannot be realized due to the reciprocity condition, the 3-port passive duplexer has to be lossy. This inherent loss affects both the TX insertion loss ($TXIL$) and the noise figure (NF). Another configuration of this lossy duplexer has four ports, where the added port is used to model the loss simplifying the analysis by dealing with 4-port lossless passive S-matrix [82]. This extra port is called the balance (BAL) port as seen in Fig. 4.2(b).

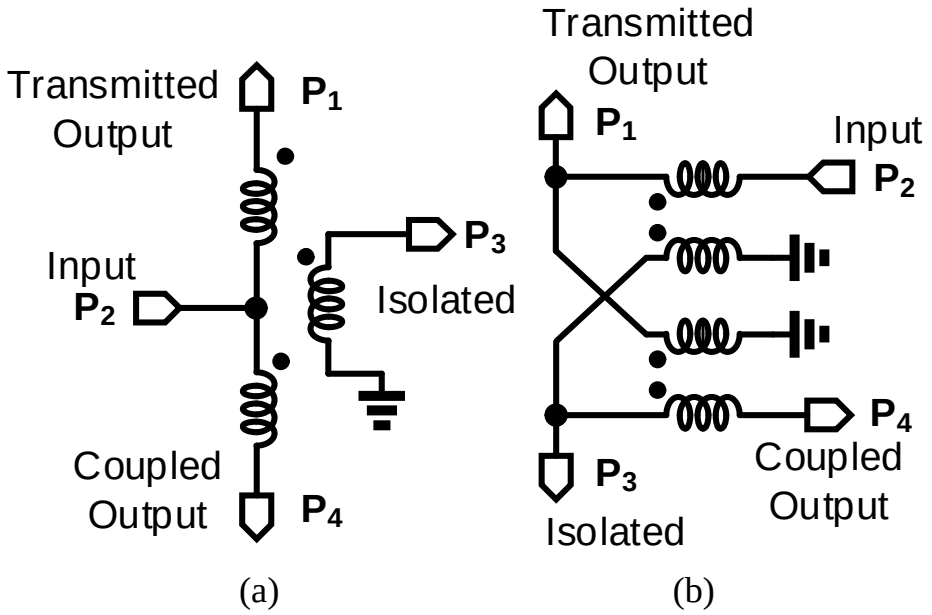


Figure 4.3: Anti-symmetric directional coupler emulated by (a) a hybrid transformer, and (b) a cross-connected transformer.

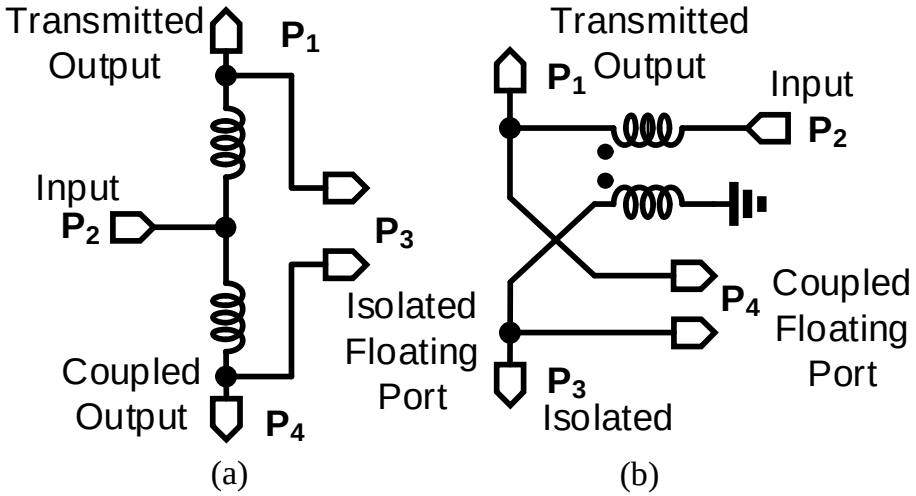


Figure 4.4: Single component emulation of anti-symmetric directional coupler with one floating port using (a) a center-tapped inductor, and (b) a single transformer.

4.2.2 Four-Port Reciprocal Duplexers

The main concept behind this type of duplexers is to divide the TX power between the ANT and the BAL ports with certain ratio r defined as the ratio of the TX signal power delivered to the ANT port divided by the TX signal power delivered to the BAL port. The scattering matrix of the 4-port passive lossless duplexer in Fig. 4.2(b) is defined by [83]:

$$S_{4p,ideal} = \frac{1}{\sqrt{1+r}} \begin{bmatrix} 0 & \sqrt{\mathrm{r}}\mathrm{e}^{-\mathrm{j}\theta} & 1\,\mathrm{e}^{-\mathrm{j}\gamma} & 0 \\ \sqrt{\mathrm{r}}\mathrm{e}^{-\mathrm{j}\theta} & 0 & 0 & 1\mathrm{e}^{-\mathrm{j}\gamma} \\ 1\mathrm{e}^{-\mathrm{j}\gamma} & 0 & 0 & \sqrt{\mathrm{r}}\mathrm{e}^{-\mathrm{j}\beta} \\ 0 & 1\mathrm{e}^{-\mathrm{j}\phi} & \sqrt{\mathrm{r}}\mathrm{e}^{-\mathrm{j}\beta} & 0 \end{bmatrix}, \tag{4.2}$$

where ANT is port 1, TX is port 2, RX is port 3 and BAL is port 4, θ, γ, ϕ and β are the phase shifts due to the delays in different paths of the duplexer. To satisfy the condition for a lossless passive scattering network, the phases should be related as follows [80]:

$$(\theta - \phi) + (\beta - \gamma) = (2\mathrm{n}_1 + 1)\ \pi, \tag{4.3}$$

where n_1 is any integer number. If there is a reflection at the ANT port ($\Gamma_{ANT} \neq 0$), a reflected TX signal at the BAL port is needed in order to cancel TX signal at the RX port, as shown in Fig. 4.2(b), satisfying the following condition:

$$\left(\Gamma_{ANT}\,\sqrt{r}\,e^{-j\theta}\right)\ e^{-j\gamma} + \left(\Gamma_{BAL}\,e^{-j\phi}\right)\ \sqrt{r}\,e^{-j\beta} = 0. \tag{4.4}$$

By applying eq. (4.3) to eq.(4.4):

$$\Gamma_{BAL} = \Gamma_{ANT}\,e^{j2(\beta-\gamma)}. \tag{4.5}$$

For this reason, this type of duplexers is called electrical balance duplexers (EBDs), since the concept of isolation is based on balancing two paths TX-ANT-RX and TX-BAL-RX to cancel each other.

The well-known directional coupler (DC) can be used as a 4-port EBD, since it has two pairs of conjugate ports. Conjugate ports are two port that are completely isolated from each other where $S_{nm} = S_{mn} = 0$ $(m \neq n)$. Two types of directional couplers can be used as 4-port EBDs: i) the symmetric one ($S_{12} = S_{34}$, $S_{13} = S_{24}$), ii) the anti-symmetric one or magic-T, (($S_{12} = -S_{34}$, $S_{13} = S_{24}$) or ($S_{12} = S_{34}$, $S_{13} = -S_{24}$)). Lumped element circuits can be used to emulate the anti-symmetric DC, as shown in Fig. 4.3, namely a hybrid transformer and a cross-connected transformer [84]. This can be further simplified using one floating port, as illustrated in Fig. 4.4. These two circuits will be studied to determine the pros and cons of possible configurations of passive EBDs. The scattering matrix of the symmetric one can be formulated as:

$$S_{DC,sym} = \frac{e^{-j\theta}}{\sqrt{1+r}} \begin{bmatrix} 0 & \sqrt{\mathrm{r}} & \pm\mathrm{j} & 0 \\ \sqrt{\mathrm{r}} & 0 & 0 & \pm\mathrm{j} \\ \pm\mathrm{j} & 0 & 0 & \sqrt{\mathrm{r}} \\ 0 & \pm\mathrm{j} & \sqrt{\mathrm{r}} & 0 \end{bmatrix}. \tag{4.6}$$

In this case, the RX signal in ANT-RX path has an extra phase shift of $\pm\pi/2$ relative to ANT-TX path. Furthermore, $\beta - \gamma = \pm\pi/2$, and $\Gamma_{BAL} = -\Gamma_{ANT}$. The scattering matrix of the anti-symmetric DC is given by:

$$S_{DC,sym} = \frac{e^{-j\theta}}{\sqrt{1+r}} \begin{bmatrix} 0 & \sqrt{\mathrm{r}} & 1 & 0 \\ \sqrt{\mathrm{r}} & 0 & 0 & \pm 1 \\ 1 & 0 & 0 & \mp\sqrt{\mathrm{r}} \\ 0 & \pm 1 & \mp\sqrt{\mathrm{r}} & 0 \end{bmatrix}. \tag{4.7}$$

In the anti-symmetric S-matrix, $\beta - \gamma = \pm\pi$ or 0, and $\Gamma_{BAL} = \Gamma_{ANT}$. Also, there is always a π phase difference between TX-BAL path and RX-BAL path.

Directional couplers are wideband and low loss, but they are bulky and cannot be integrated. Symmetric DC cannot be easily emulated using integrated lumped components, since it requires a wideband $\pi/2$ phase shifter. However, the operation of the anti-symmetric DC can be emulated using integrated hybrid [76, 77] and cross-connected transformers as shown in Fig. 4.3(a), (b), respectively. The hybrid transformer power ratio r depends on the ratio between the inductances from center-tape point, P_2, to ports P_1 and P_4, while in case of the cross-connected transformer it is determined by the turn-ratios and the coupling factors of the transformers [85].

In order to simplify the design of the integrated low noise amplifier (LNA), the RX port is not matched. The port is usually capacitive or open circuit to have maximum voltage at the input of the LNA. This can be modeled as $a_{RX} = b_{RX}$, where b_{RX} is the reflected wave at RX port and a_{RX} is the incident wave at RX port, since all the power at the RX port is reflected back. Assuming $\theta = 0$ in (4.7) for simplicity, the S-matrix of the three remaining ports can be calculated using:

$$\begin{bmatrix} \mathrm{b_{ANT}} \\ \mathrm{b_{TX}} \\ \mathrm{b_{BAL}} \end{bmatrix} = \begin{bmatrix} 1 & \sqrt{\mathrm{r}} & \frac{\mp\sqrt{\mathrm{r}}}{\sqrt{1+\mathrm{r}}} \\ \sqrt{\mathrm{r}} & 0 & \mp 1 \\ \frac{\mp\sqrt{\mathrm{r}}}{\sqrt{1+\mathrm{r}}} & \mp 1 & \frac{\mathrm{r}}{\sqrt{1+\mathrm{r}}} \end{bmatrix} \begin{bmatrix} \mathrm{a_{ANT}} \\ \mathrm{a_{TX}} \\ \mathrm{a_{BAL}} \end{bmatrix} \tag{4.8}$$

where a_{ANT}, a_{TX} and a_{BAL} refer to the incident (input) waves andb_{ANT}, b_{TX} and b_{BAL} refer to the output waves. From (4.8), ANT and BAL ports are no longer conjugates and the return loss at the ANT becomes a function of r. In case $\Gamma_{BAL} = \Gamma_{ANT}$, TX and RX ports are conjugate and $TXIL$ is the same for both cases of the matched and the open circuit RX port.

4.2.3 Practical Configurations

The hybrid transformer and the cross-connected transformer have two pairs of terminals called conjugate pairs ($P_1 - P_4$ and $P_2 - P_3$), as shown in Fig. 4.4. A conjugate pair forms two terminals that are isolated form each other. Since the EBD is a 4-port device of paired ports, there will be four different port configurations for each structure. Due to the symmetry of the structures in Fig. 4.3, only two unique configurations are available for each transformer structure. As a result, there are two possible configurations using the hybrid transformer, where the TX and the RX ports are exchanged, and two possible configurations using **a** cross-connected transformer, where the ANT and the BAL ports are exchanged.

4.2.3.1 Floating RX

This is the default EBD configuration reported in [76–78, 86, 87]. As described in Fig. 4.5, the TX port is the center-tap of the hybrid transformer in Fig. 4.4(a). To achieve the matching condition ($\Gamma_{BAL} = \Gamma_{ANT}$), the balancing impedance must satisfy:

$$Z_{BAL} = r\, Z_{ANT} \tag{4.9}$$

The TX signal is common-mode for ANT and BAL ports, while the RX signal is the difference between ANT and BAL ports. Since the ANT and the BAL ports have the same TX voltage, this duplexer is called voltage-mode EBD. In this configuration, the RX port can be considered as a floating port between the ANT and the BAL ports. To eliminate the high voltage common-mode signal, a transformer is used as difference detector. The receiver insertion loss ($RXIL$) profile is optimum at the resonance between L_2 and C_{LNA}, while the passband from the TX port to the

ANT and BAL ports has a low-pass response. This circuit achieves low transmitter insertion loss ($TXIL$), since the PA is directly connected to the antenna, but it has two main drawbacks: i) the RX signal is attenuated due to transformer coupling loss from the ANT port to the LNA, ii) the common-mode TX signal at the input of the LNA is relatively large due to the capacitive coupling of the transformer, where the attenuation or common-mode rejection ratio ($CMRR$) depends on the parasitic coupling capacitance (C_C). The $CMRR$ can be calculated using:

$$CMRR = 20 \log_{10}\left(\frac{C_C}{C_{LNA}}\right) \tag{4.10}$$

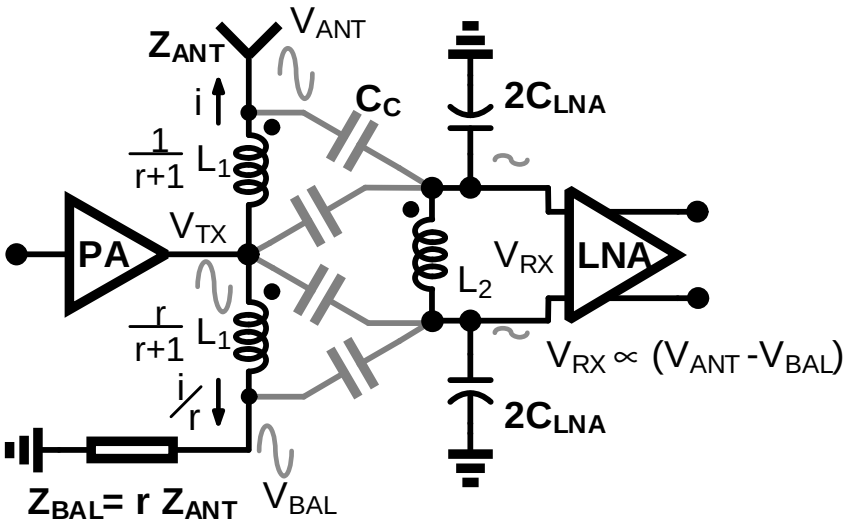


Figure 4.5: An EBD with a floating RX port (voltage-mode EBD) [82].

The second drawback was addressed in [77, 78] using a fully differential version of this duplexer. However, this necessitates adding an extra balun at the ANT port. This extra balun degraded $TXIL + RXIL$ by 1-2 dB. Another solution is recently

proposed in [87] by grounding one side of secondary winding, where a single-ended LNA is used instead of the differential LNA. The effect of coupling C_C is canceled at RX port by extra capacitance parallel to Z_{BAL}.

4.2.3.2 Floating TX

Another duplexer configuration is realized by exchanging the PA and the LNA of the first configuration as shown in Fig. 4.6. The difference between ANT and BAL voltages is proportional to the TX voltage, while the TX port is floating. Unlike the floating RX configuration, where ANT and BAL ports have the same voltage, the floating TX configuration is characterized by a TX current flowing through ANT and BAL ports with the same magnitude but opposite direction, as seen in Fig. 4.6. Thus, this circuit is called a current-mode EBD. Since the PA and LNA were exchanged in this configuration, the transfer function from TX to ANT will be a band-pass around the resonance frequency of L_2 and C_{PA}, while the transfer function from ANT to RX will be a low-pass. By applying $\Gamma_{BAL} = \Gamma_{ANT}$, the condition for TX-RX isolation is given by:

$$Z_{BAL} = Z_{ANT}/r \tag{4.11}$$

Since the two impedances Z_{BAL} and Z_{ANT} have the same TX current (i), then the voltage at the balance impedance $V_{BAL} = -i\,Z_{BAL} = -i\,Z_{ANT}/r$, while the voltage at the antenna $V_{ANT} = i\,Z_{ANT}$. This means $V_{BAL} = -V_{ANT}/r$. This is an advantage in this configuration, since the balancing network has a lower voltage. The lower voltage V_{BAL} means simpler switch design in Z_{BAL} compared to the floating RX configuration . Another advantage of this configuration, when used with on-chip power amplifiers, is the ability to merge the transformer with the power combiner of the PA to decrease the losses in the transformer. On the other hand, the main

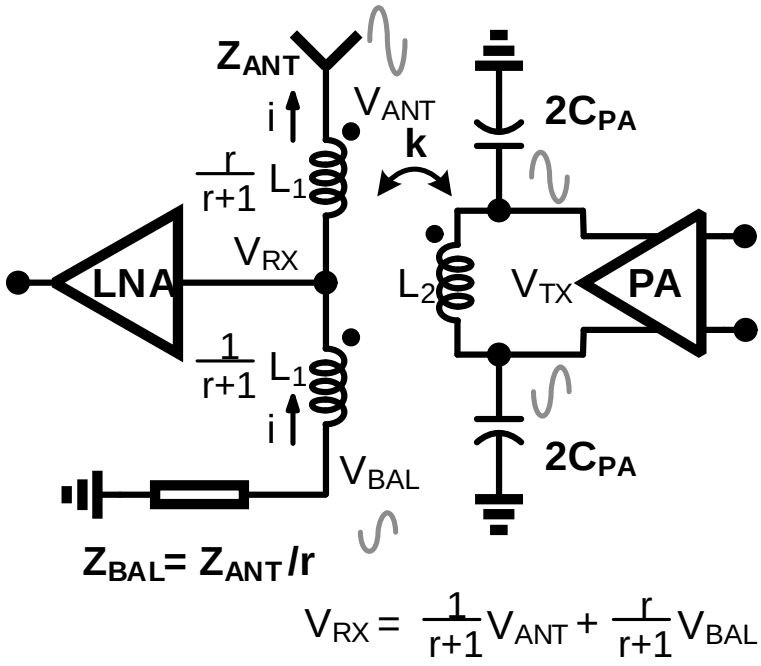


Figure 4.6: An EBD with a floating TX port (current-mode EBD).

drawbacks of this circuit are the higher $TXIL$ due to the coupling losses of the transformer and the higher NF due to increased LNA noise. The increase in the NF is due to the low voltage RX signal at the LNA input, which causes higher effect of LNA noise on the total NF.

4.2.3.3 Floating ANT

This configuration is different from the previous configurations, since it is based on emulating an anti-symmetric directional coupler by a cross-connected transformer (see Fig. 4.4(b)) instead of the hybrid transformer. The PA is connected to the input port, while the LNA is connected to the isolated port, as shown in Fig. 4.7. Because of the orientation of the antenna relative to the RX port, the RX signal has an extra π phase shift. Since Z_{BAL} and Z_{ANT} have the same TX voltage, then they are related by $\mathrm{Z_{BAL}} = r\, Z_{ANT}$ to satisfy the TX-RX isolation condition. Consequently,

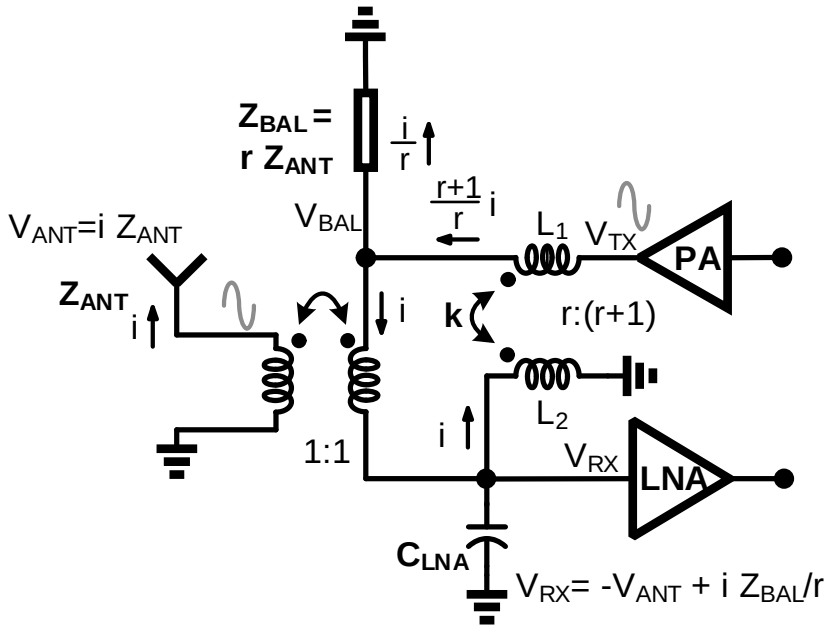


Figure 4.7: An EBD with a floating ANT port. The antenna in nature is relative to ground, thus a balun is required between the antenna and the duplexer.

this circuit has the same balancing condition as the floating RX configuration in Fig. 4.5. In this circuit, r depends on the turn ratio of the transformer connected to the TX port and the coupling factor k of this transformer [84, 85]. A second transformer with $(1:1)$ ratio is required to convert the single-ended voltage across the ANT port to a floating voltage and vice-versa. This added transformer degrades both $TXIL$ and NF and limits the use of this configuration.

4.3 Proposed EBD with Floating Z_{BAL}

4.3.1 Floating Z_{BAL} Configuration

Based on the cross-connected transformer topology, a fourth configuration is realized in this work. By swapping ANT and BAL ports of the third configuration, the BAL port will be floating with no need for a balun. The proposed circuit, shown in Fig. 4.8, employs a floating Z_{BAL} to ensure wideband operation. The condition

of the isolation is defined by $Z_{BAL} = r\,Z_{ANT}$. The proposed circuit has four main advantages: i) there is no common-mode TX signal at the input of the single-ended LNA. Consequently, this duplexer can support higher power operation without compromising the LNA linearity performance, ii) a relatively large voltage RX signal is achieved at the LNA input minimizing the effect of the LNA noise on the total NF, iii) the ANT port is directly connected to the TX port, since there is nearly no TX voltage drop across the transformer between the two ports, iv) there is a direct path between ANT port and RX port through Z_{BAL} without degradation due to transformer coupling loss. However, these advantages come at the cost of the increased design complexity. First, the balance ratio r in this configuration depends on the coupling factor of the transformer (k), which can be alleviated using accurate electromagnetic (EM) simulation of the transformer to determine r. Additionally, the design of a tunable floating balancing network Z_{BAL} that supports high power operation is very challenging. This issue will be addressed in detail in sub sections 4.4.3 and 4.4.4.

4.3.2 TXIL and RXIL Analysis

The insertion loss of duplexers is very crucial since it highly affects the total power efficiency of the transmitter and the sensitivity of the receiver. For ideal lossless passive EBDs (Fig. 4.2(b)), the TX power is divided between the ANT and BAL ports and RX power is divided between BAL and ANT ports. Thus, $TXIL$ and $RXIL$ can be determined by:

$$TXIL = -10\,\log_{10}\left(\frac{P_{TX-ANT}}{P_{TX}}\right) = 10\,\log_{10}\left(\frac{r+1}{r}\right) \tag{4.12}$$

$$RXIL = -10\,\log_{10}\left(\frac{P_{RX-ANT}}{P_{RX}}\right) = 10\,\log_{10}\left(r+1\right) \tag{4.13}$$

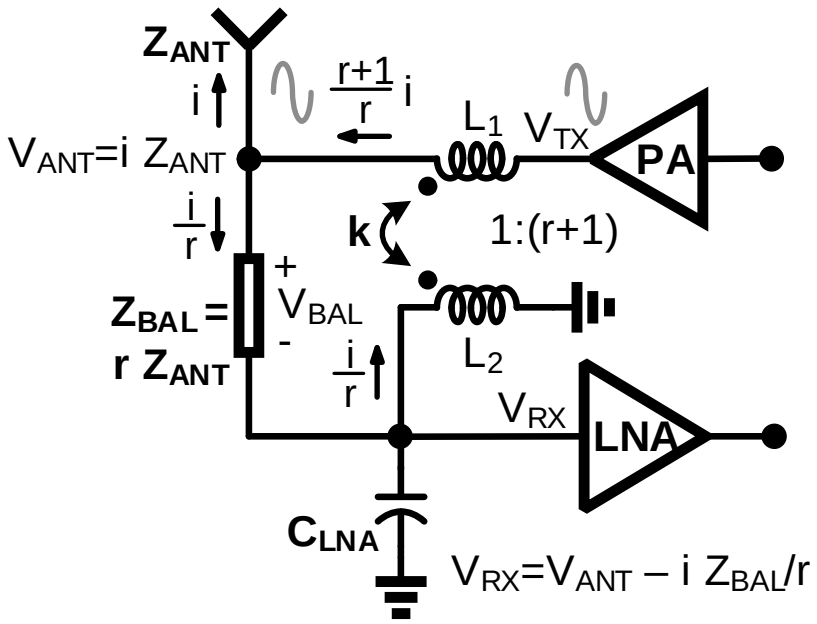
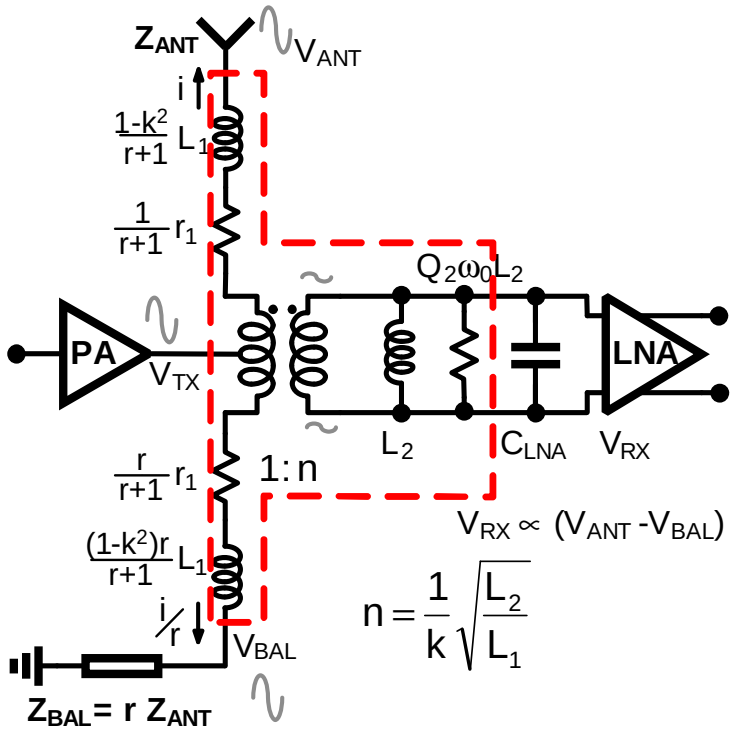


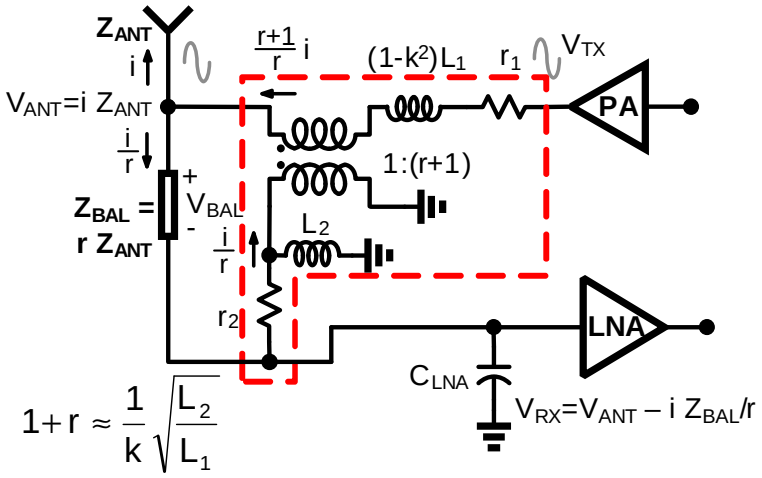
Figure 4.8: The proposed EBD with a floating balancing network (BAL) port alleviates the problem of common-mode TX signal at LNA input in [76].

Transformer loss effect is not accounted in (4.12) and (4.13), since they describe $TXIL$ and $RXIL$ of a lossless passive 4-port EBDs. Transformer loss affects $TXIL$ and $RXIL$ of the four aforementioned configurations differently. The $TXIL$ and $RXIL$ of the proposed configuration (Fig. 4.8) are analyzed and compared to the first configuration depicted in Fig. 4.5. In both configurations, the transformer is replaced by its equivalent circuit model, which is an ideal transformer with parasitic self-inductances and resistances, as shown in Fig. 4.9. Since the TX and RX ports are conjugate, the RX port is set as a short circuit without affecting $TXIL$ to simplify the analysis. $TXIL$ of the first and fourth configurations are given by:

$$TXIL_{C1} = 10\ \log_{10}\left(\frac{1+r+r_1/R}{r}\right) \tag{4.14}$$



(a)



(b)

Figure 4.9: (a) First configuration (floating RX) and (b) Forth configuration (floating Z_{BAL}), where the transformer is replaced by its equivalent circuit ($Q_2 = \omega_0 L_2/r_2$).

$$TXIL_{C4} = 10\,\log_{10}\left(\frac{1+r}{r\,\rho^2}\right) \tag{4.15}$$

where

$$\frac{1}{\rho^2} = \left(1 + \frac{r_1\,(1+r) + \omega_0\,L_2/\,(1+r)\,Q_2}{r\,R}\right) \tag{4.16}$$

and r_1 is a series resistances to model the loss in primary L_1, while Q_2 models loss of secondary turn L_2 at the frequency ω_0 and R is the resistance of the antenna. By comparing (4.14) and (4.15), $TXIL$ of both configurations are close to each other, since r_1 and r_2 are very small compared to R. The derivation of (4.14) and (4.15) is explained in detail in section 4.3.3.

Similarly, TX port can be replaced by an open circuit without affecting the transfer function from ANT to RX to simplify the $RXIL$ analysis. Using Fig. 4.9, $RXIL$ of configuration 1 is found to be:

$$RXIL_{C1} = 10\,\log_{10}\left(\frac{1+r+r_1/R}{\sigma^2}\right) \tag{4.17}$$

where

$$\frac{1}{\sigma^2} = \left(1 + \frac{(1+r)\,R + r_1}{k^2\,Q_2\,\omega_0\,L_1}\right) \tag{4.18}$$

and k is the transformer coupling factor. σ models the extra $RXIL$ due to the loss in the secondary coil of the hybrid transformer in Fig. 4.9(a). $RXIL$ of configuration 4 can be calculated by:

$$RXIL_{C4} = 10\,\log_{10}\left(\frac{1+r}{\psi^2}\right) \tag{4.19}$$

where

$$\frac{1}{\psi^2} = \left(1 + \frac{R\,(1+r)}{Q_2\,\omega_0\,L_2}\right). \tag{4.20}$$

Equations (4.17) and (4.19) are also derived in section 4.3.3. ψ is used to model the

effect of the loss in the secondary coil illustrated in Fig. 4.9(b). By comparing (4.17) and (4.19), $RXIL_{C4}$ of the proposed configuration is lower than $RXIL_{C1}$, because of the $1/k^2$ factor in σ definition which is not present in ψ definition.

4.3.3 Detailed $TXIL$ and $RXIL$ Analysis

To derive (4.14) and (4.15), the RX ports in Fig. 4.9 can be considered as a short circuit, because TX and RX ports are conjugate ports. Fig. 4.10(a) and (b) show the circuit after reduction of RX port. Furthermore, the reactive elements can be removed at the frequency of operation, because their effect will be canceled at the matching port impedance to be simplified to Fig. 4.10(c) and (d).

For configuration 1 in Fig. 4.10(c), the rms voltage at TX port $V_{TX,rms}$ can be calculated by:

$$V_{TX,rms} = \sqrt{P_{TX}\, R_{TX}} = \sqrt{P_{TX}\, \left(\frac{r}{r+1}\right)\left(R + \frac{r_1}{r+1}\right)}, \tag{4.21}$$

where R_{TX} is the TX port resistance, P_{TX} is the TX input power at the duplexer and R is R_{ANT}. Therefore, the rms voltage at ANT port:

$$V_{ANT,rms} = V_{TX,rms}\, \frac{R}{R + r_1/\left(r+1\right)} = \sqrt{P_{ANT,TX} R}. \tag{4.22}$$

From (4.21) and (4.22):

$$TXIL_{C1} = 10\, \log_{10}\left(\frac{P_{TX}}{P_{ANT,TX}}\right) = 10\, \log_{10}\left(\frac{1 + r + r_1/R}{r}\right) \tag{4.23}$$

which is the same as (4.14).

For configuration 4 in Fig. 4.10(d), the rms voltage at TX port $V_{TX,rms}$ can be

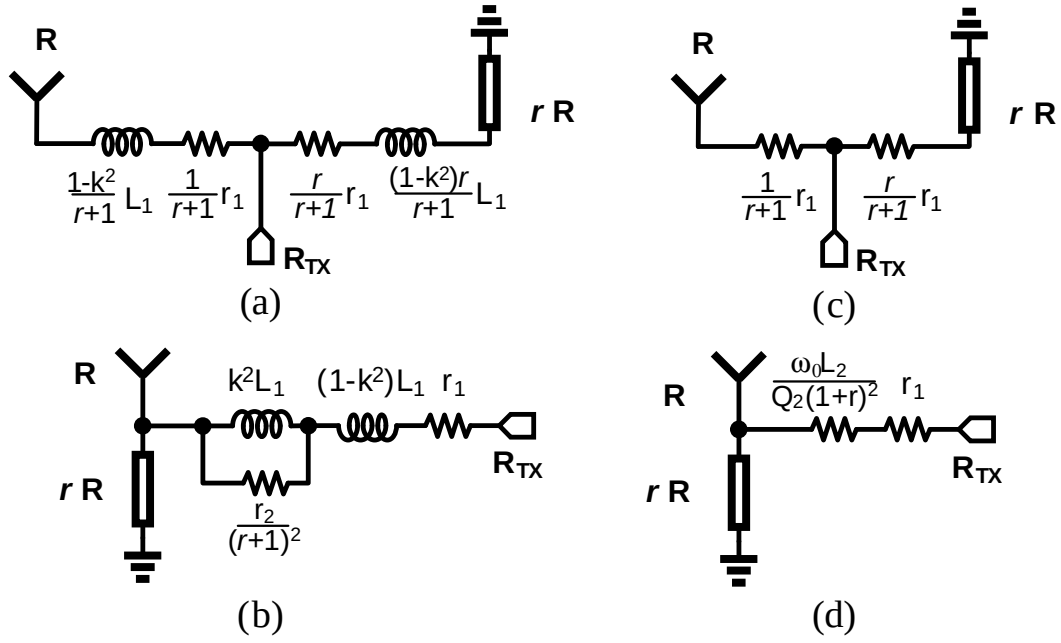


Figure 4.10: Circuit model (a) for calculating TXIL in config. 1, (b) for calculationg TXIL in config. 4, (c) simplified of (a), (d) simplified of (d).

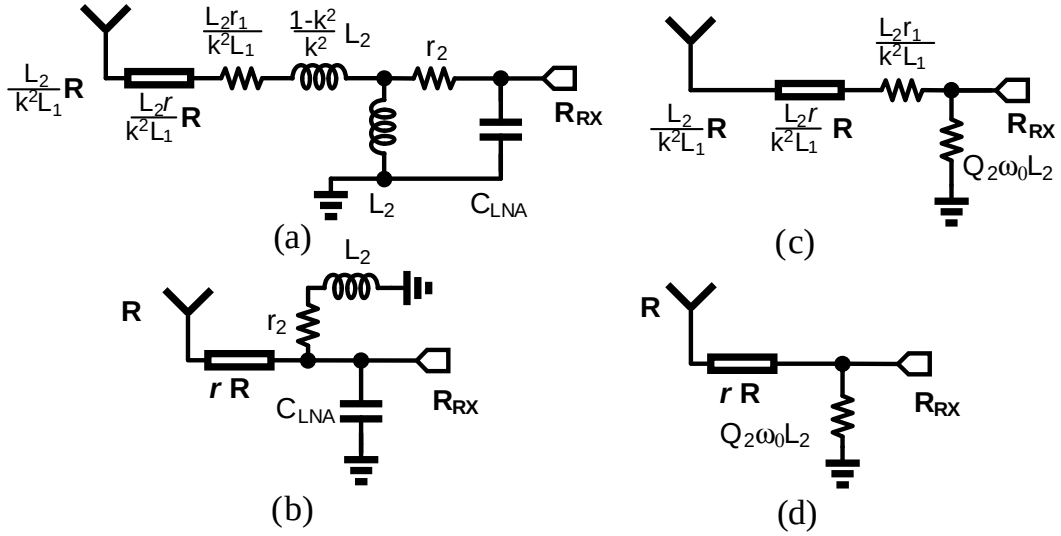


Figure 4.11: Circuit model (a) for calculating RXIL in config. 1, (b) for calculationg RXIL in config. 4, (c) simplified of (a), (d) simplified of (d).

calculated by:

$$V_{TX,rms} = \sqrt{P_{TX}\, R_{TX}} = \sqrt{P_{TX}\left(\frac{r\, R}{r+1} + r_1 + \frac{\omega_0 L_2}{Q_2\,(r+1)^2}\right)}. \tag{4.24}$$

Therefore, the rms voltage at ANT port:

$$V_{ANT,rms} = \sqrt{P_{ANT,TX} R} = \frac{V_{TX,rms}\, r\, R}{r\, R + (1+r)\, r_1 + \omega_0 L_2 / Q_2 (1+r)} \tag{4.25}$$

(4.15) can be derived from (4.24) and (4.25).

For calculating RXIL, the TX port in Fig. 4.9 is assumed to be an open circuit, since the RX and TX are conjugate ports. The circuit models in 4.9 are simplified to the circuit models in 4.11(a) and (b). In Fig. 4.11(a), the leakage inductance in series with the antenna is neglected since it is in series with a much larger impedance. At high values of L_1, this leakage inductance cannot be neglected increasing RXIL than the one predicted by expression. Fig. 4.11(a) and (b) can be further simplified at the resonance frequency of L_2 and C_{LNA}, as shown in Fig. 4.11(c) and (d). Since the ANT port is not matched because TX port is open circuit, RXIL is defined as $R_{RX}/P_{ANT,RX}$. For configuration 1 in Fig. 4.11(c), the rms voltage at the RX port is defined by:

$$V_{RX,rms} = \sqrt{P_{RX}\, R_{RX}} \approx \sqrt{P_{RX}\left(\frac{Q_2 \omega_0 L_2\, R_{eq}}{Q_2 \omega_0 L_2 + R_{eq}}\right)}, \tag{4.26}$$

where

$$R_{eq} = \frac{L_2}{k^2\, L_1}\left(R\,(1+r) + r_1\right). \tag{4.27}$$

The rms voltage at the ANT port due to the RX signal is calculated by:

$$V_{ANT,rms} = \sqrt{P_{ANT,RX}\, \frac{R\, L_2}{k^2\, L_1}} = V_{RX,rms}\, \frac{R\, L_2 / k^2\, L_1}{R_{eq}}. \tag{4.28}$$

From (4.26) and (4.28):

$$RXIL_{C1} = 10\,\log_{10}\left(\left(1 + r + \frac{r_1}{R}\right)\left(1 + \frac{R_{eq}}{Q_2\omega_0 L_2}\right)\right) \tag{4.29}$$

which is the same result as in (4.17).

For configuration 4 in Fig. 4.11(d), the rms voltage at RX port $V_{RX,rms}$ can be calculated by:

$$V_{RX,rms} = \sqrt{P_{RX}\,R_{RX}} \approx \sqrt{P_{RX}\left(\frac{Q_2\omega_0 L_2\,(1+r)\,R}{Q_2\omega_0 L_2 + (1+r)\,R}\right)}. \tag{4.30}$$

Therefore, the rms voltage at ANT port:

$$V_{ANT,rms} = \sqrt{P_{ANT,RX}R} = \frac{V_{RX,rms}}{1+r}, \tag{4.31}$$

where (4.19) can be derived from (4.30) and (4.31).

4.3.4 Noise Analysis

Noise figure (NF) of a passive circuit is the same as its $RXIL$; however, considering the noise due to the LNA, the cascaded NF of the EBD and the LNA is higher than $RXIL$ and depends on EBD configuration. Assuming LNA input impedance is capacitive (C_{LNA}) which resonates with the inductor L_2, NF can be modeled at the resonance frequency by the following equation:

$$NF = 10\,\log_{10}\left(\frac{1}{|S_{31}|^2} + \frac{\bar{v}^2_{n,LNA}}{|A_V|^2\;4\,k_B\,T\,B\,R}\right) \tag{4.32}$$

where A_V is the voltage gain from the ANT noise source to LNA input, S_{31} is the S-parameter from ANT to RX where its magnitude is the inverse of $RXIL$, R is the antenna resistance, $\bar{v}^2_{n,LNA}$ is the input voltage referred noise of the LNA, γ is the effective noise factor of input MOS devices, B is the noise bandwidth. Assuming

LNA noise is dominated by input devices of the LNA, $\bar{v}_{n,LNA}^2$ can be modeled by $4\,k_B\,T\,B\,\gamma/G_{m,eff}$, where $G_{m,eff}$ is the effective transconductance of the LNA input devices. Using the scattering matrix of anti-symmetric directional couplers by setting $\Gamma_{RX} = 1$ [85], A_V can be determined by:

$$|A_V| = \left|\frac{V_{RXS}}{V_S}\right| = |S_{31}|\sqrt{\frac{R_{RX}}{R}} \tag{4.33}$$

where V_S is the voltage source that models the RX signal at the antenna, V_{RXS} is the voltage at RX port due to V_S, and R_{RX} is the resistance seen at RX port when $\Gamma_{BAL} = \Gamma_{ANT}$. A_V and R_{RX} for each configuration are shown in Table 4.1. Thus NF is described as:

$$NF = RXIL + 10\,\log_{10}\left(1 + \frac{\gamma}{G_{m,eff}\,R_{RX}}\right) \tag{4.34}$$

The value of R_{RX} depends on the configuration and can be found by setting TX port open or short circuit and analyzing the circuit at the frequency of resonance of L_2 with C_{LNA}. So for configuration 1, when TX port is open circuit, $R_{RX-C1} \approx (1+r)\,R\,L_2/k^2L_1$. Similarly, for configuration 4, when TX port is an open circuit, $R_{RX-C4} \approx (1+r)\,R$. While, for configuration 2, when TX port is a short circuit, $R_{RX-C2} \approx R\,/(1+r)$. Therefore, the first and fourth configurations have small added NF due to the LNA while the second configuration is highly affected due to the small value of R_{RX}.

4.3.5 Comparison Among Different Configurations

Table 4.1 summarizes a comprehensive analysis for the four passive EBD configurations. In order to verify the analysis, the four configurations are designed and simulated using different values of r, but with fixed values of L_2, $C_{LNA} = C_{PA}$ (or resonance frequency of L_2 =5.4 nH and C_{LNA} =1.3 pF at f_0 =1.9 GHz), and $G_{m,eff}$.

Table 4.1: Analysis Comparison Among the Four Different Passive EBD Configurations

	Configuration 1	**Configuration 2**	**Configuration 3**	**Configuration 4**
R_{RX}/R^* (Ω/Ω)	$\approx \frac{(1+r)}{k^2}\frac{L_2}{L_1}$	$\approx \frac{1+r\,r_1/R(1+r)}{1+r}$	$\approx (1+r)$	$\approx (1+r)$
$\lvert A_V \rvert$ (V/V)	$\approx \frac{\sigma}{k}\sqrt{\frac{L_2}{L_1}}$	$\approx \frac{1}{1+r}$	$\psi \times 10^{IL_B/10}$	ψ
TXIL (dB)	$10\log_{10}\left(\frac{1}{r}\left(1+r+\frac{r_1}{R}\right)\right)$	$10\log_{10}\left(\frac{1}{r\sigma'^2}\left(1+r+\frac{r\,r_1}{R}\right)\right)$	$10\log_{10}\left(\frac{1+r}{r\rho'^2}\right)+IL_B$ **	$10\log_{10}\left(\frac{1+r}{r\rho^2}\right)$
RXIL (dB)	$10\log_{10}\left(\frac{1}{\sigma^2}\left(1+r+\frac{r_1}{R}\right)\right)$	$10\log_{10}\left(1+r+\frac{r\,r_1}{R}\right)$	$10\log_{10}\left(\frac{1+r}{\psi^2}\right)+IL_B$ **	$10\log_{10}\left(\frac{1+r}{\psi^2}\right)$
NF-RXIL (dB)	$10\log_{10}\left(1+\frac{k^2L_1}{(1+r)L_2}\frac{\gamma}{RG_{m,eff}}\right)$	$10\log_{10}\left(1+\frac{(1+r)\gamma}{(R+r_1r/(1+r))G_{m,eff}}\right)$	$10\log_{10}\left(1+\frac{\gamma}{(1+r)RG_{m,eff}}\right)$	$10\log_{10}\left(1+\frac{\gamma}{(1+r)RG_{m,eff}}\right)$

*** The transformer is considered lossless except for configuration 2 to simplify expression**

** IL_B is the loss due to the balun between the antenna and the duplexer

σ' is similar to σ but with r is replaced by $1/r$ & ρ' is similar to ρ but with dividing Q_2 by r^2

Also, the coupling factor of the transformer is fixed for this comparison (k =0.75). The loss of the transformer is modeled by a series resistance on each branch where $Q_1 = \omega_0 L_1/r_1$ and $Q_2 = \omega_0 L_2/r_2$. For comparison purpose, Q_1 and Q_2 are assumed to be fixed ($\sim$ 15). To change r in the first and second configurations, the point of center-tape is shifted to change the division of power ratio between ANT and BAL ports. L_1 was chosen to minimize the sum of $TXIL$ and $RXIL$ using the following:

$$L_{1opt,C1} \approx \frac{R}{\omega_0}\,(1+r)\,\sqrt{\frac{Q_1}{2.2\,k^2\,Q_2}} \tag{4.35}$$

$L_{1opt,C1}$ is the optimum L_1 value to provide the minimum$TXIL + RXIL$ for the first configuration calculated from (4.14) and (4.17). $L_{1opt,C2}$ will be the same as $L_{1opt,C1}$, but r needs to be replaced by $1/r$. Fig. 4.12 shows that the analysis results of $TXIL + RXIL$ almost match the simulation results for different r values of the first configuration. The discrepancy for large L_1 values is due to two sources of errors: i) simplification in $RXIL$ expression of the first configuration (or $TXIL$ expression of the second configuration) as illustrated in section 4.3.3, ii) reflections at TX and RX ports which increase $TXIL$ and $RXIL$ respectively. For the fourth (and third) configurations, L_1 value is controlled by the ratio r and can be calculated directly from L_2 and r by:

$$L_{1,C4} = \frac{L_2}{k^2\,(1+r)^2} \tag{4.36}$$

For NF comparison, a fixed $G_{m,eff}$ of 80 mS is used for all configurations with γ = 1 for short-channel effect. As shown in Fig. 4.13, the analytical expressions almost match simulation results. Clearly, for all configurations, as r increases the duplexer $TXIL$ is improved at the expense of NF degradation. The NF in configuration 4 is better than NF in configuration 1 by 0.5 dB for $r > 1.5$. The NF of configuration 2

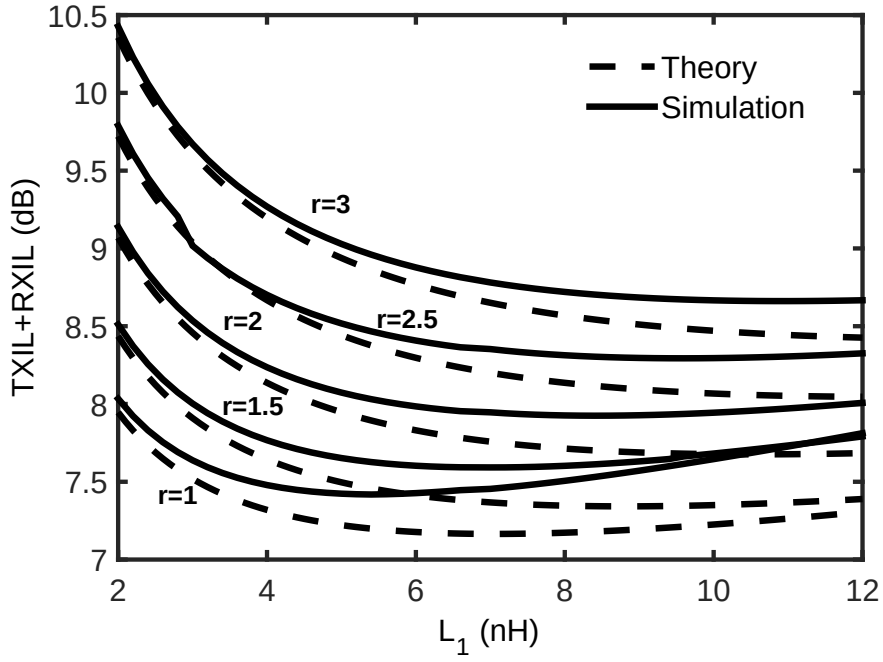


Figure 4.12: Comparison between $TXIL + RXIL$ calculated by the theoretical expression and by simulation in configuration 1.

is higher than the other configurations due to its low R_{RX} as depicted in Fig. 4.13(c). Configuration 4 is compared against configuration 3, as shown in Fig. 4.13(b) and (d). Both configurations have almost the same NF, but $TXIL$ of configuration 4 is slightly lower for $r > 1$ and $TXIL$ of configuration 3 is slightly lower for $r < 1$.

4.4 Circuit Implementation

A prototype is implemented in 0.18μm CMOS technology to verify the operation of the proposed EBD configuration with floating Z_{BAL} [79]. It operates in a frequency range of 1.6-2.2 GHz. This section discusses the circuit implementation details of the duplexer and is divided into five sub-sections describing the main blocks of the prototype including transformer, LNA, and balancing impedance network. The fourth sub-section demonstrates the impact of Z_{BAL} non-idealities on NF and

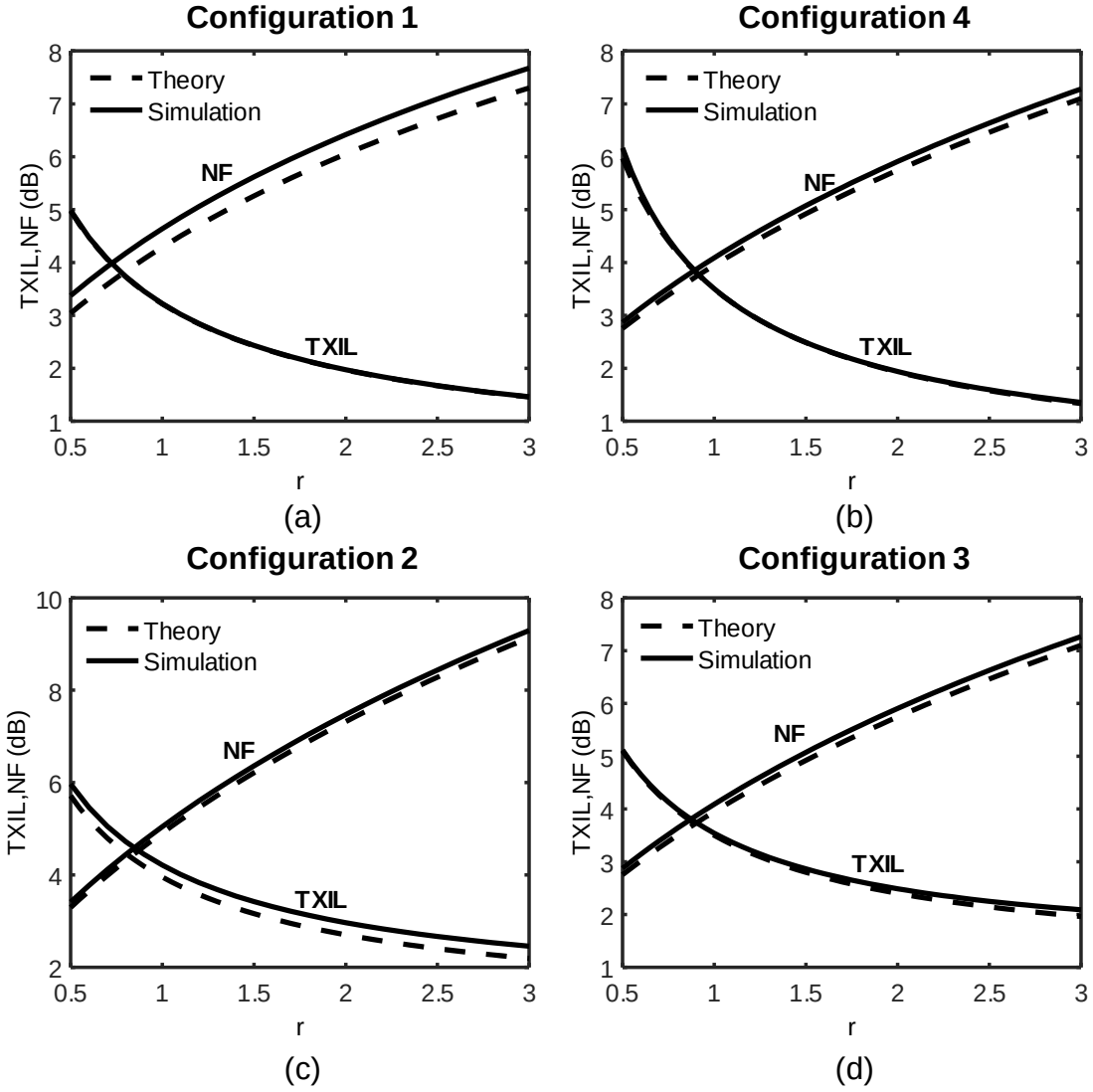


Figure 4.13: Comparison between $TXIL$ and NF in (a) configuration 1 using optimized L_1, (b) configuration 4, (c) configuration 2 using optimized L_1, (d) configuration 3 without considering the balun loss.

linearity performance, while the last section describes the effect of switch-induced Z_{BAL} modulation on the linearity performance.

4.4.1 Transformer

The transformer is initially designed for a power ratio of r =1.45 to achieve about 3 dB $TXIL$ with acceptable NF. The primary side has one turn while the secondary side has two turns. The transformer is designed with an outer dimension of 484 μm, and a 5 μm metal spacing using the thick top aluminum layer of 0.18 μm CMOS process. The thickness of the top metal (M6) is 4 μm which improves the transformer quality factor. The underneath connections are made with three thin metal layers (M3-M5) to decrease the connection resistance without too much added parasitic capacitance.

The layout of the transformer is shown in Fig. 4.14, where the routing to TX (or PA) and ANT pads is included in the EM simulation, since it affects the overall performance. EM simulation was performed using Sonnet to accurately model the transformer properties especially the ratio r. From EM simulation, L_1 =1.83 nH, L_2 =3.62 nH and $|k|$ =0.61. k seems relatively small considering a tightly wound interwound transformers ($\sim$ 0.8) due to the extra routing from the pads to the winding. Using the model in Fig. 4.9(b), the calculated r = 1.31. The slight change from the designed value r =1.45 is due to the extra routing from the transformer to the pads. The quality factor of L_1 (Q_1) and the quality factor of L_2 (Q_2) variations with frequency are shown in Fig. 4.15. These results are for ANT and PAGND ports connected to ground, and measuring the impedance at TX and RX ports.

4.4.2 LNA

The LNA is designed using a complementary common-source low noise transconductance amplifier (LNTA) with G_m =70 mS ($G_m = g_{mp}+g_{mn}$) and a drain resistance

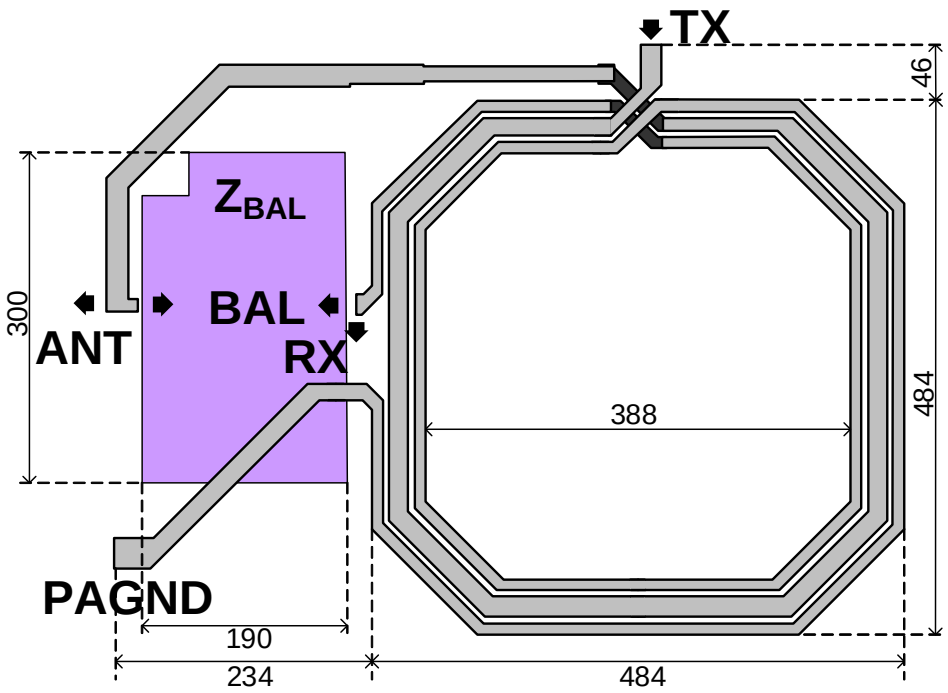


Figure 4.14: Layout of transformer, L_1 =1.83 nH (width W_1 =18 μm) contains the middle turning, L_2 =3.62 nH (width W_2 =10 μm) contains both outer and inner turnings and the spacing between the turns is 5 μm (all the provided dimensions in the figure are in micons).

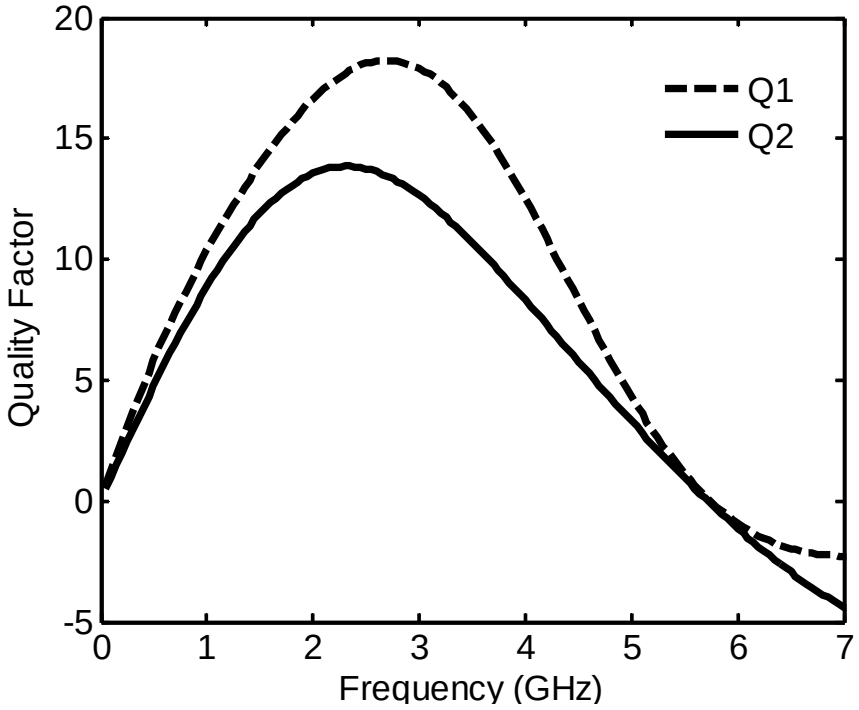


Figure 4.15: Simulated transformer quality factor as a function of frequency.

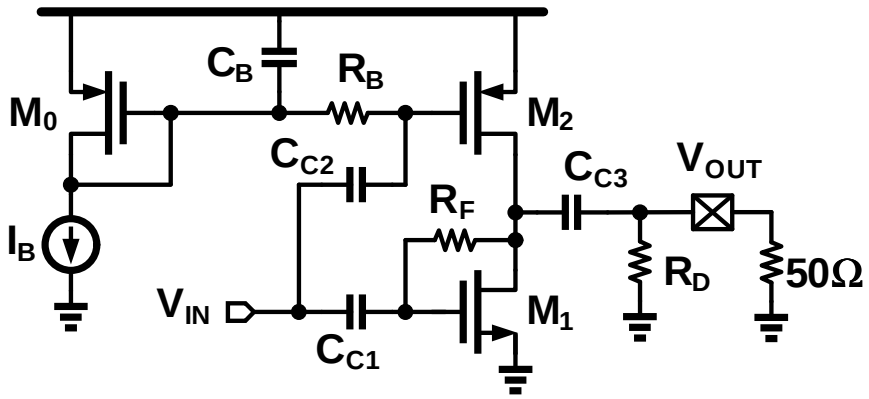


Figure 4.16: Schematic of the LNA.

(R_D =70 Ω), as shown in Fig. 4.16. The output matching is achieved without the need for an external buffer. The use of PMOS and NMOS devices increases G_m/I_d

while a large overdrive voltage enhances the linearity performance of the LNA. The LNA current is controlled by the current mirror M_0-M_2 and I_B, while the output dc voltage equals to $V_{gs,M1}$. R_F is used only for dc biasing of the drain of M_1 and M_2, thus its value was chosen to be higher than 10 kΩ to preserve the high input impedance at V_{IN}. Another advantage of this topology is its wide band operation, since it is inductorless. The resonance frequency at the input can be changed by varying the capacitance at V_{IN} to increase the operating range.

4.4.3 Balancing Impedance

The radiation impedance of a typical planar inverted-F antenna (PIFA) used in cellular handsets varies slowly as the near-field of the antenna is perturbed. Recently, an antenna tuning circuitry has been used to compensate for the antenna impedance variations to present more stable impedance for the PA [88]. The *balancing impedance* should track the residual antenna impedance variation within the bandwidth of interest to achieve the required TX-RX isolation. Moreover, for multi-band operation, Z_{BAL} needs to be tuned to achieve the required isolation in each band. The design of Z_{BAL} has three challenges: high power operation, floating impedance, and wide tuning range with fine steps for an acceptable range of antenna impedance variation. High power operation mandates stacking of thick gate devices, where triple-well 3.3V NMOS devices were used to arbitrarily control the bias of the bulk. Since the TX signal will be higher than 10 Vpp, the bulk should be carefully biased to avoid the forward bias of the drain/source diodes during negative excursions of the TX signal. Therefore, the bulks of the switches are biased at -1 Vdc when the switches are off while it is biased 0 Vdc when the switches are on. The gates and bulks are biased through level shifters and buffers that convert the digital control word to (3V/-1V) for gate biasing and (0V/-1V) for bulk biasing.

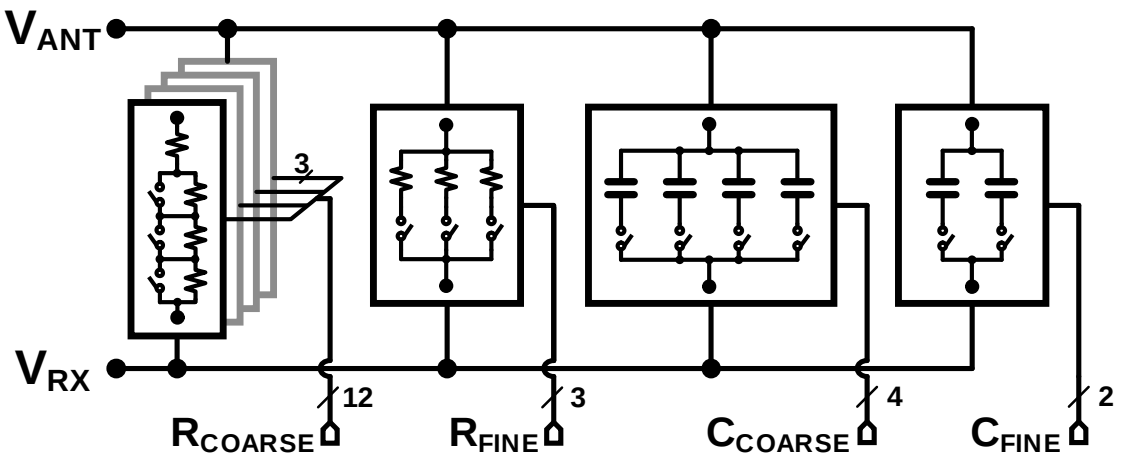


Figure 4.17: RC network for Z_{BAL} implementation.

The implementation of the programmable RC floating impedance network with minimum RX signal loss through the parasitics of switches is extremely challenging. To minimize the effect of these parasitics while achieving fine tuning steps, the design of the RC network is divided into coarse and fine sections for both R and C components, as shown in Fig. 4.17. Resistance coarse tuning is achieved using a series network with 3-bit control as shown in Fig. 4.18(a) to provide a wide tuning range of 43-121 Ω. R_g and R_b are large resistances ($\sim$ 90 kΩ) to minimize their effect on NF. This network is replicated four times with parallel connection and independent control to achieve the required range of resistance with minimum parasitics. The layout diagram of the course resistor cell is depicted in Fig. 4.18(c). Fine resistance tuning is realized by a 3-bit control of parallel resistors with stacked switches to provide 0.5 Ω fine tuning steps. A capacitor bank with coarse/fine tuning is designed to provide a wide tuning range of 600 fF and fine resolution of 10 fF. Furthermore, the course tuning element C in Fig. 4.18(b) also represents the stacked switches used to enable TX high power operation. The tolerated normalized antenna admittance is shown

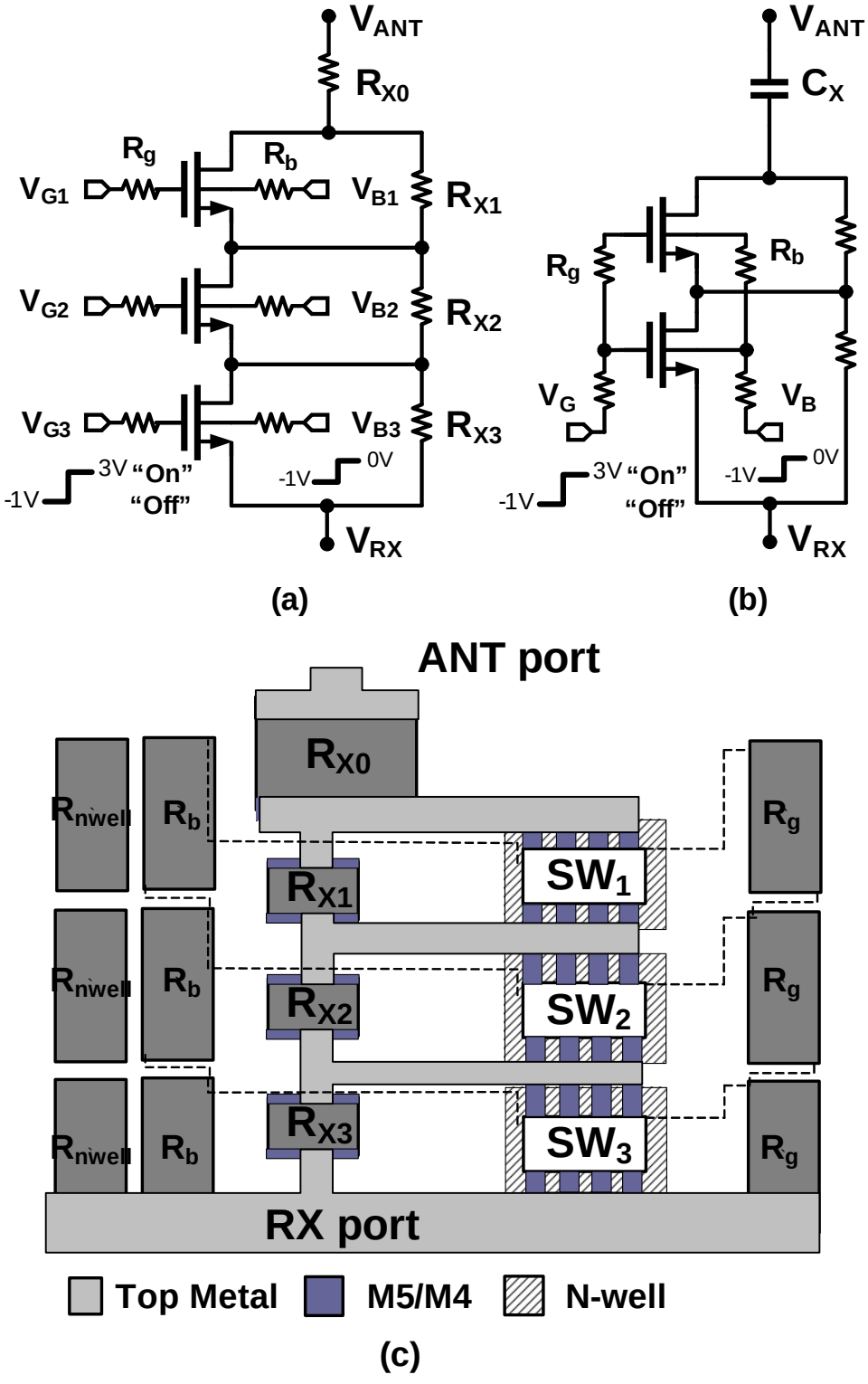


Figure 4.18: (a) Schematic of the balancing resistance coarse tuning element, (b) schematic of the capacitive coarse tuning element, (c) layout diagram of a resistive coarse tuning element (area 85×55 μm^2).

in Fig. 4.19. In practice, an antenna tuning unit (ATU) is required to convert the wide variation of the antenna impedance within VSWR≈3 to the tolerated range of VSWR≈1.3 - 1.5 [89, 90]. As depicted in Fig. 4.19, an extra capacitance tuning is needed to support the ANT impedance within VSWR≈1.5 at 1.8 GHz. Since only the reactive part of the tolerated ANT admittance range is affected by frequency, the tolerated admittance range in Fig. 4.19 will slightly decrease at 1.6 GHz and slightly increase at 2.2 GHz.

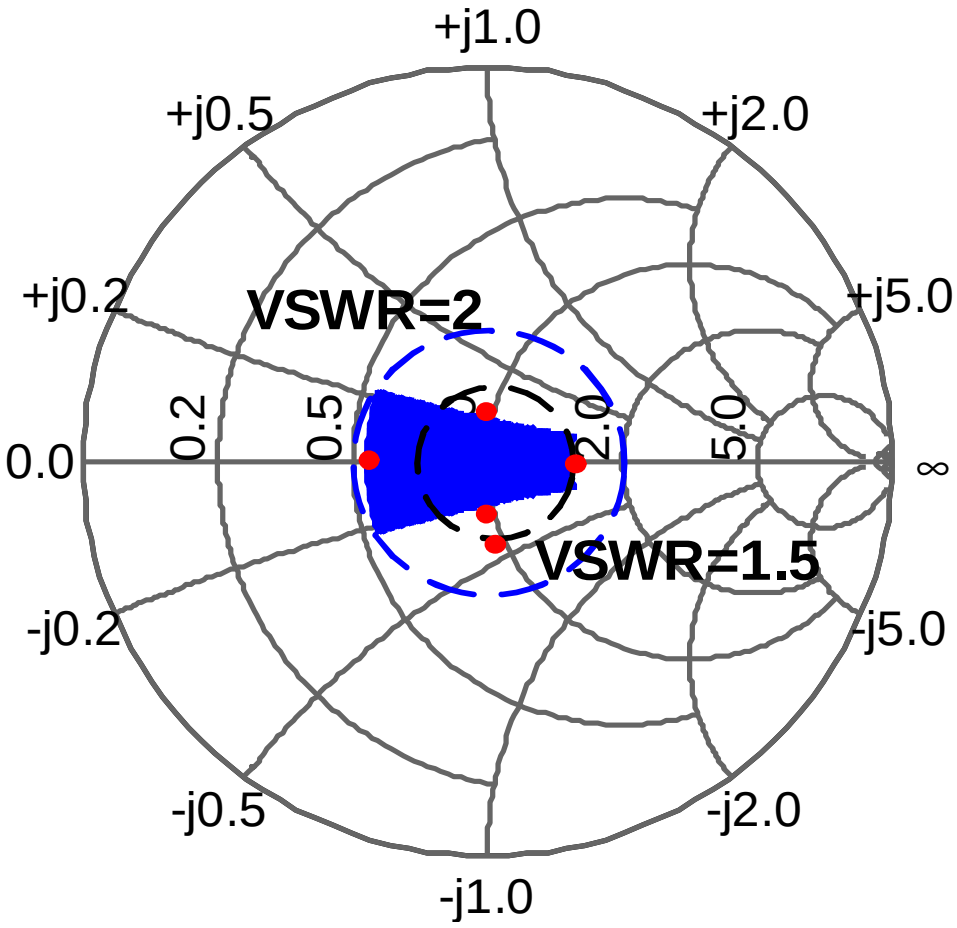


Figure 4.19: Supported antenna admittance normalized to 20mS at 1.8GHz, where blue points represent the covered range of shunt R-C of Z_{BAL}, and red dots represent post-layout simulation.

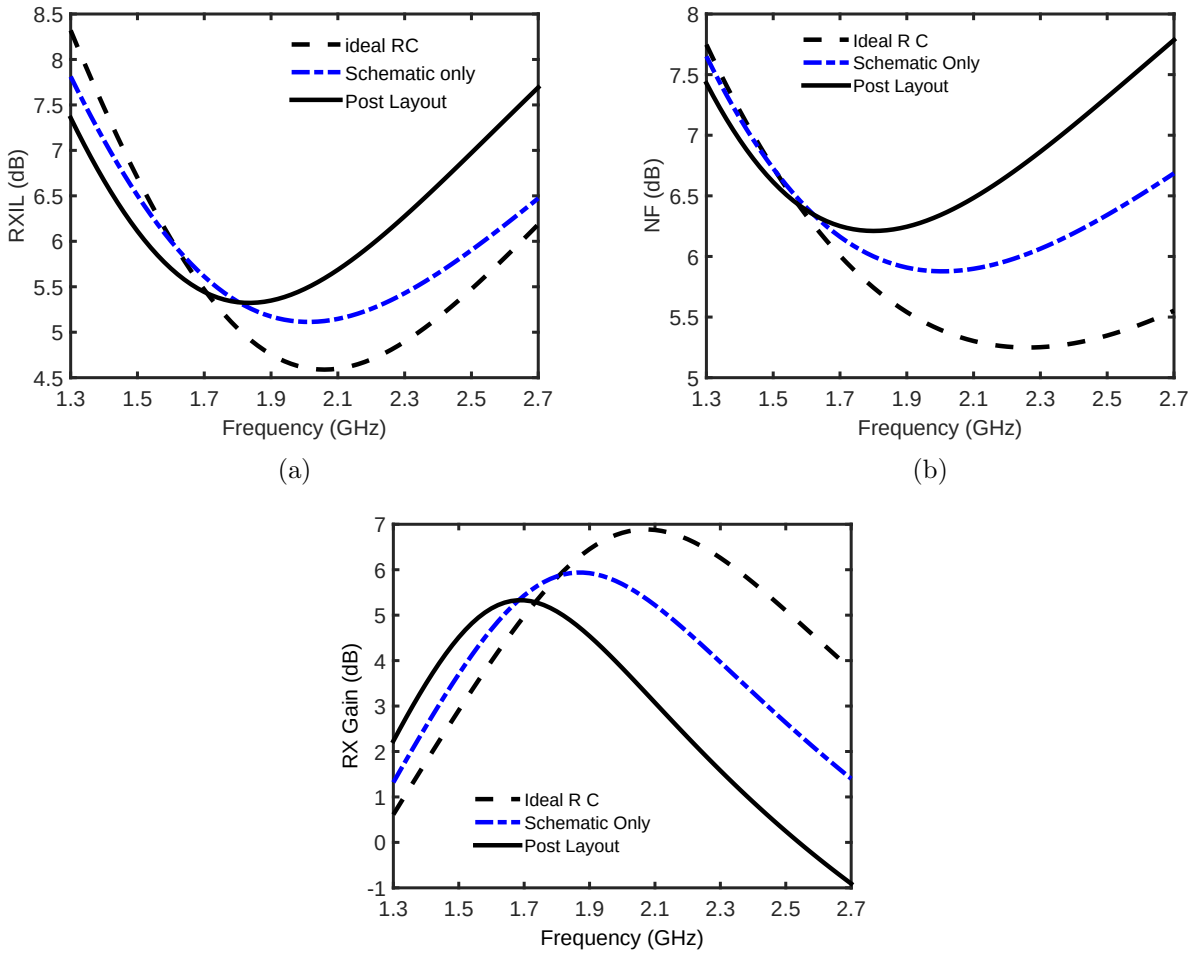


Figure 4.20: Effect of tunable Z_{BAL} on (a) $RXIL$ (EBD only) (b) Cascaded NF (EBD and LNA) (c) RX gain (EBD and LNA).

4.4.4 Impact of Z_{BAL} Non-idealities on NF and Linearity

To assess the effect of the parasitics due to the tunable Z_{BAL} on EBD $RXIL$ and the cascaded NF, the duplexer is simulated with an ideal R-C then compared to the NF with the implemented tunable Z_{BAL} including the switches (schematic only and post-layout), as shown in Fig. 4.20(a) and (b). The minimum $RXIL$ increased from 4.6 dB to 5.35 dB, while the minimum NF increased from 5.22 dB to 6.21

dB. The increase in NF is attributed to RX signal loss due to switches parasitics (see Fig. 4.20(a) and (c)), and the resistors used in switches biasing. The layout of the tunable resistors and capacitors is optimized to minimize the parasitics as illustrated in Fig. 4.18(c), where the top metal layers are used for routing with width proportional to the expected currents to pass. Furthermore, very thin wires are used to connect R_g and R_b to the gates and the bulks of the switches, respectively. The sizes of the switches and the resistors in Fig. 4.18(c) are designed to support the highest occurring current, when the switches are all "on". The sizes of the switches (Fingers = 12, W =5 μm, W =0.4 μm) are optimized to minimize the increase in $RXIL$.

For the ideal RC case in Fig. 4.20(b), the minimum NF equals to 5.22 dB. The main contributors to noise from simulation are: i) R_{ANT} 28.9 %, ii) R_{BAL} 38.9 %, iii) transformer 11.4 %, iv) LNA (including R_D) 20.4 %. The LNA adds only 0.9 dB to the cascaded NF which is expected to decrease by using advanced CMOS technologies with smaller feature size compared to 0.18 μm. At 2.25 GHz (where NF is minimum), Q_1 =17 and Q_2 =13.5, or r_1 =1.5 Ω and r_2 =3 Ω. Using (4.15) and (4.19), $TXIL$ =2.77 dB and $RXIL$ =4.47 dB, where r = 1.31 and R =50 Ω. The theoretical NF is calculated using (4.34) to be 4.97 dB, where $R_{RX} \approx (1+r)\, R_{ANT} \approx 117\Omega$, $\gamma \approx 1$ and $G_{m,eff} \approx 70mS$. The difference between theoretical and simulated NF is only 0.25 dB. This difference is mainly because of the resistive load of the LNA which is not included in the NF expression.

The impact of the switches on NF can be significantly reduced by using a silicon on insulator (SOI) technology, since there is no need for isolation resistances to bias the bulk. However, the excess noise due to the gate biasing resistances is still present. Furthermore, the SOI technology has minimum parasitic nonlinear substrate capacitance that reduces harmonic distortion [87]. In circuit level, to break the trade-off

between the number of stacked transistors affecting NF and linearity performance, a transformer can be used to convert the floating BAL port into a differential Z_{BAL} with two impedance networks referenced to ground. The transformer may limit the bandwidth of TX-RX isolation, which can be alleviated by using a wide bandwidth transformer and a dual-notch balancing network similar to [87, 91].

Since there is a direct trade-off between the number of stacked devices in the balancing network and NF, only two stacked devices were used to switch capacitances, as shown in Fig. 4.18(b). The implemented course tunable resistance shown in Fig. 4.18(a) suffers from a degraded linearity, when $V_{G1} = -1\,V$, $V_{G2} = 3\,V$ and $V_{G3} = 3\,V$. The linearity of switches is affected mainly by two mechanisms when the switch is off, namely conduction and breakdown. Assume there are two RF signals with amplitudes A_1 and A_2 at the switch drain and source terminals respectively as shown in Fig. 4.21. To prevent conduction, V_{GS} has to be less than the threshold voltage $V_{th,NFET}$ (~ 0.7 Vdc). The maximum $V_{GS} = \Delta A/2 - 1\,V$ occurs at the peaks of the RF signal, where $\Delta A = A_1 - A_2$ is the difference in voltage amplitude at drain and source terminals. Therefore, ΔA is limited to 3.4 V. Similarly for the bulk connection to avoid forward biased diodes, ΔA is also limited to 3.4 V. Assuming drain-gate and drain-bulk breakdown voltages of 3.6 V, the maximum tolerable ΔA before the breakdown is 5.2 V. Consequently, the linearity of Z_{BAL} is limited by the conduction mechanism (through drain/source or drain/bulk) not breakdown. The linearity is verified by simulating the balancing network to have $IIP3 = 43.5\,dBm$ for Z_{BAL} setting that introduces the highest intermodulation. This linearity performance is reasonable to verify the operation of the proposed topology and can be enhanced in future work using a differential Z_{BAL} implementation.

The intermodulation between a received blocker and the TX signal is very critical in the evaluation of the duplexer linearity performance. Since Z_{BAL} is floating, the

received blocker signal at ANT port propagated to RX port modulates the value of Z_{BAL}. The third order intermodulation ($IM3$) of the blocker signal and TX signal is high in the case of floating Z_{BAL}. The differential Z_{BAL} implementation can significantly improve the $IM3$ performance, as it does not suffer from the trade-off between NF and linearity, and three stacked devices or more can be used to implement the switches. Additional improvement in linearity is achieved by using a fixed resistive load while a tunable C-L-C matching π-network is used to change the effective input resistance [87]. Since Z_{BAL} is not a function of the blocker signal, the $IM3$ of the blocker and TX signals is enhanced.

4.4.5 Switch-Induced Z_{BAL} Modulation

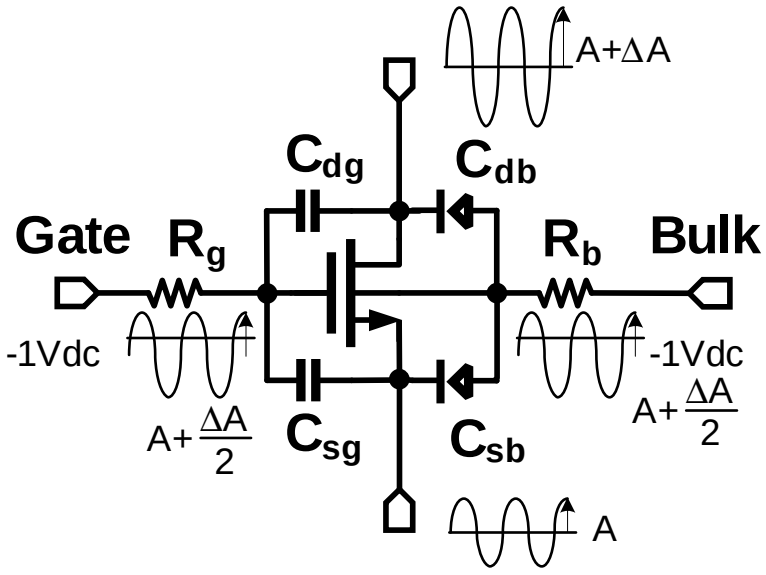


Figure 4.21: Schematic diagram of a switch unit in the off state.

The non-linear behavior of Z_{BAL} due to conduction mechanism of the switches in a stacked structure can be modeled by studying the relation between the conduction

current (i_{ds}) of a single NMOS switch and the voltage applied on it in the off-state. When the switch is off, the current (i_{ds}) is a non-linear function of drain/source voltage difference (v_{ds}):

$$i_{ds} \approx I_{s1} \exp\left(\frac{V_G + v_{ds}/2}{nV_T}\right) + I_{s2}\left[\exp\left(\frac{V_B - v_{ds}/2}{nV_T}\right) - 1\right] \tag{4.37}$$

where the first term is due to the sub-threshold conduction current and the second term is due to the conduction current through the bulk-drain diodes. I_{s1} is the sub-threshold current at $V_{GS} = 0$, n the is slope factor, V_G is the dc bias of the gate, I_{s2} is the reverse-biased current of the diode, V_B is the bulk dc voltage, and V_T is the thermal voltage. Using Taylor expansion, i_{ds} can be approximated as:

$$i_{ds} \approx g_1 v_{ds} + g_2 v_{ds}^2 + g_3 v_{ds}^3 \tag{4.38}$$

where g_1, g_2 and g_3 are the conductance parameters:

$$g_1 \approx \frac{I_{s1}}{2nV_T} \exp\left(\frac{V_G}{nV_T}\right) - \frac{I_{s2}}{2V_T} \exp\left(\frac{V_B}{V_T}\right) \tag{4.39}$$

$$g_2 \approx \frac{I_{s1}}{(2nV_T)^2} \exp\left(\frac{V_G}{nV_T}\right) - \frac{I_{s2}}{(2V_T)^2} \exp\left(\frac{V_B}{V_T}\right) \tag{4.40}$$

$$g_3 \approx \frac{I_{s1}}{(2nV_T)^3} \exp\left(\frac{V_G}{nV_T}\right) - \frac{I_{s2}}{(2V_T)^3} \exp\left(\frac{V_B}{V_T}\right) \tag{4.41}$$

By assuming $\mathrm{V_B} = V_G$, the excess non-linear current (Δi) passing through switch can be found:

$$\Delta i = g_2 v_{ds}^2 + g_3 v_{ds}^3 \approx \exp\left(\frac{V_G}{V_T}\right) \left[\frac{v^2}{(2NV_T)^2}\left(\frac{I_{s1}}{n^2} + I_{s2}\right) + \frac{v^3}{(2NV_T)^3}\left(\frac{I_{s1}}{n^3} - I_{s2}\right)\right] \tag{4.42}$$

where v is the voltage across the stacked switches during off-state ($v = Nv_{ds}$) which is nearly the same voltage difference across Z_{BAL} and N is the number of stacked switches. The non-linear balancing network admittance (Y_{BAL}) can be expressed as:

$$Y_{BAL} = Y_0 \left(1 + y_1 v + y_2 v^2\right) \tag{4.43}$$

where Y_0 is the small signal admittance, while y_1 and y_2 are the first and second order non-linear coefficients of Y_{BAL}. y_1 and y_2 are strong functions of V_G and N. y_1 generates $HD2$ and $IM2$ distortion close to dc, while y_2 generates $HD3$ and $IM3$ distortion. It is very crucial to reduce y_2 since it defines $IIP3$ and TX-signal blocker intermodulation at the band of interest. Since y_1 and y_2 are directly proportional to g_2 and g_3 respectively, the $IIP3$ of $\mathrm{Z_{BAL}}$ can be calculated by:

$$IIP3(Z_{BAL}) \approx \sqrt{\left|\frac{4}{3y_2}\right|} \propto N\, V_T \exp\left(\frac{-V_G}{2V_T}\right) \sqrt{\left|\frac{V_T n^3 Y_O}{I_{s1} - n^3 I_{s2}}\right|} \tag{4.44}$$

The analysis reveals the behavior of Z_{BAL} $IIP3$, which is increased as the number of stacked devices N increases. The $IIP3$ is also increased by decreasing the dc voltages of the gates and the bulks of the switches.

4.5 Measurement Results

The proposed duplexer and LNA, shown in Fig. 4.8, are implemented using 0.18μm CMOS technology [79]. They occupy an active area of less than 0.35 mm^2. The die photograph is shown in Fig. 4.22. The LNA draws 7 mA from 1.5 V supply. The printed circuit board (PCB) is implemented using FR4 material and four metal layers, where the two intermediate layers were assigned for ground planes. The traces between the PA, ANT and V_{out} pins to the SMA connectors are designed to be a 50Ω transmission line (width = 14 mil, separation = 10 mil). The losses of the traces ($\sim$ 0.2 dB at 2 GHz) were de-embedded using two transmission lines (TLs)

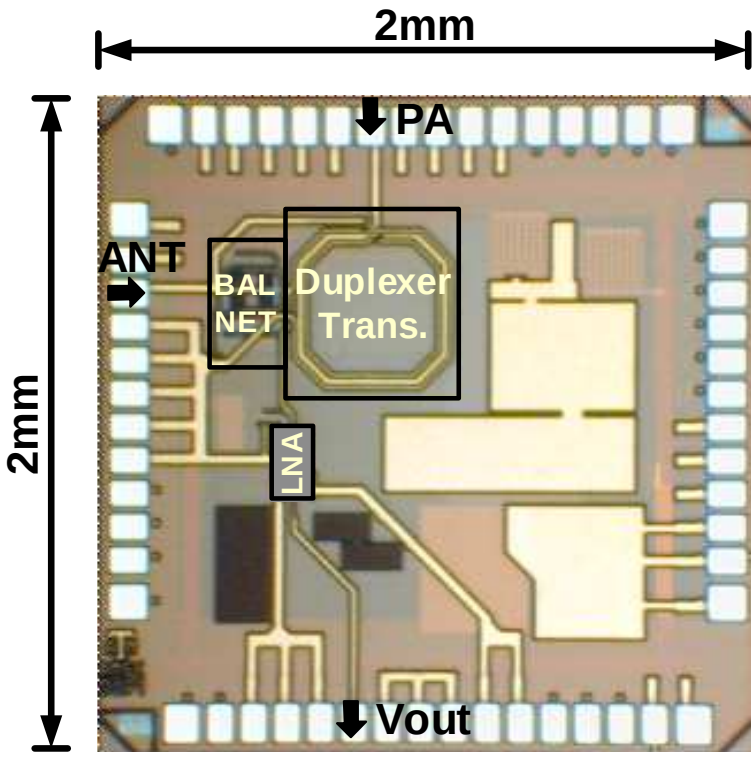


Figure 4.22: Die micrograph.

of the same length as PA-ANT trace and ANT-V_{out} trace. For NF measurement, a high gain low NF (<1.5 dB) amplifier is added after the output V_{out} to amplify the output noise by 30 dB to minimize the effect of the input noise of the spectrum analyzer. Fig. 4.23 shows the simulated and measured results of $TXIL$ and NF of cascaded duplexer and LNA using Agilent network analyzer N5230A and Agilent spectrum analyzer E4446A. The $TXIL$ is between 2.8-3.4 dB after de-embedding losses of PCB traces, while the minimum cascaded NF range is between 6.3-6.8 dB in 1.6-2.2 GHz frequency range.

Since the implemented balance ratio r is about 1.31, the input resistance seen at the PA port of the chip is close to $r\,R_{ANT}/\,(r+1)$ or 29 Ω. However, this port is required to match to 50Ω off-chip TL. An off-chip matching network is implemented

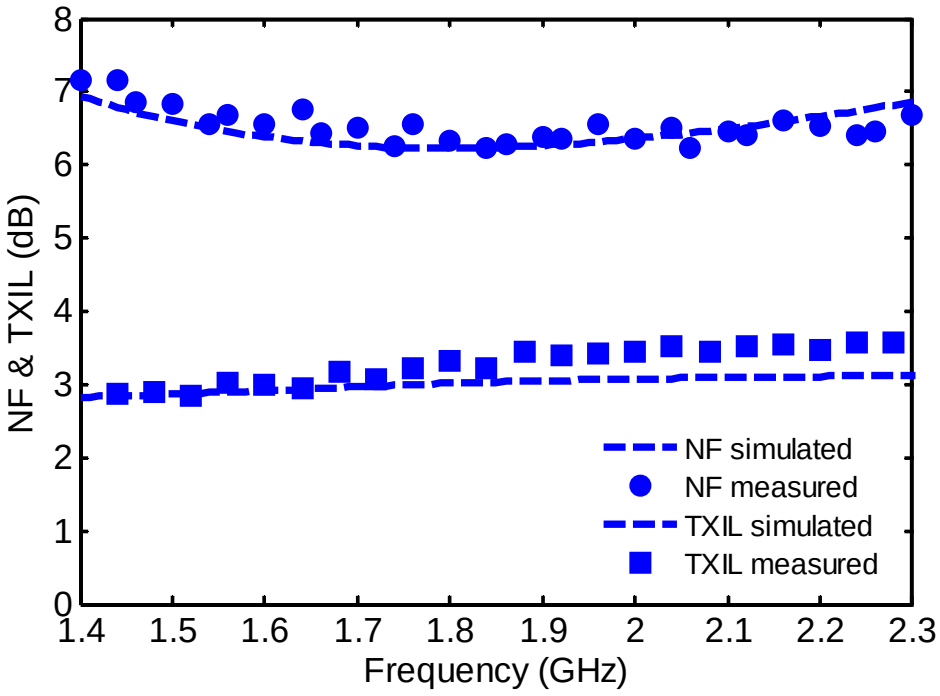


Figure 4.23: Measured TX insertion loss and noise figure of the cascaded duplexer and LNA.

in the TX side to transform the 29Ω to 50Ω using the on-chip series inductance of the duplexer and taking into account the bondwire inductance. The measured S_{22} (TX port) is less than -13 dB over the required range of 1.6-2.2 GHz, as shown in Fig. 4.24. Theoretically at the point of maximum isolation, the ANT port should have the maximum of $S_{11} \approx -10 \log_{10}(r+1)$ or -7.3 dB, when the RX port is open circuit (at the resonance frequency of L_2 and C_{LNA}). However, due to the losses of L_2, the measured S_{11} (ANT port) is less than -12 dB in the frequency range of 1.6-2.2 GHz, as depicted in Fig. 4.24. The measured TX to RX isolation for multiple balancing network settings are overlaid in Fig. 4.25. If the notch frequency is adjusted to the center of the TX band, more than 60 dB of isolation is achieved. For a maximum duplex frequency spacing of 190 MHz required by IMT band, the

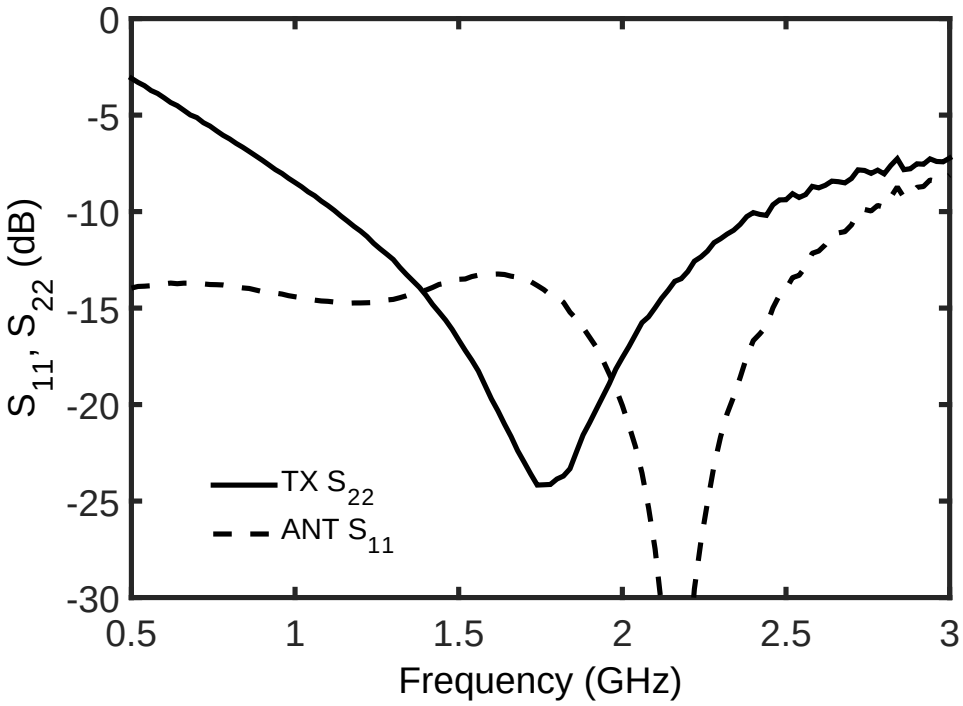


Figure 4.24: Measured PA return loss and ANT return loss.

isolation in RX band is better than 40 dB (for $R_{ANT} = 50\Omega$). The effect of Z_{ANT} variation on TX-RX isolation is shown in Fig. 4.26(a) and (b), where the minimum isolation BW (isolation < -40 dB) is 180 MHz for a 50Ω resistive load with a parallel inductance of 12.5 nH (VSWR ~ 1.42). Furthermore, shunt capacitance at ANT is balanced by tuned shunt capacitance at Z_{BAL}, where TX-RX isolation bandwidth remains unchanged, and the balancing condition is applied on a wider frequency range. Inductive has the minimum TX-RX isolation bandwidth since Z_{BAL} has a capacitive tuned element to compensate the inductance.

Pure resistive antenna impedance has the widest bandwidth of TX-RX isolation as shown in Fig. 4.26(a). Inductive Z_{ANT} has the minimum TX-RX isolation bandwidth, since Z_{BAL} has capacitive tuned element to compensate the inductance.

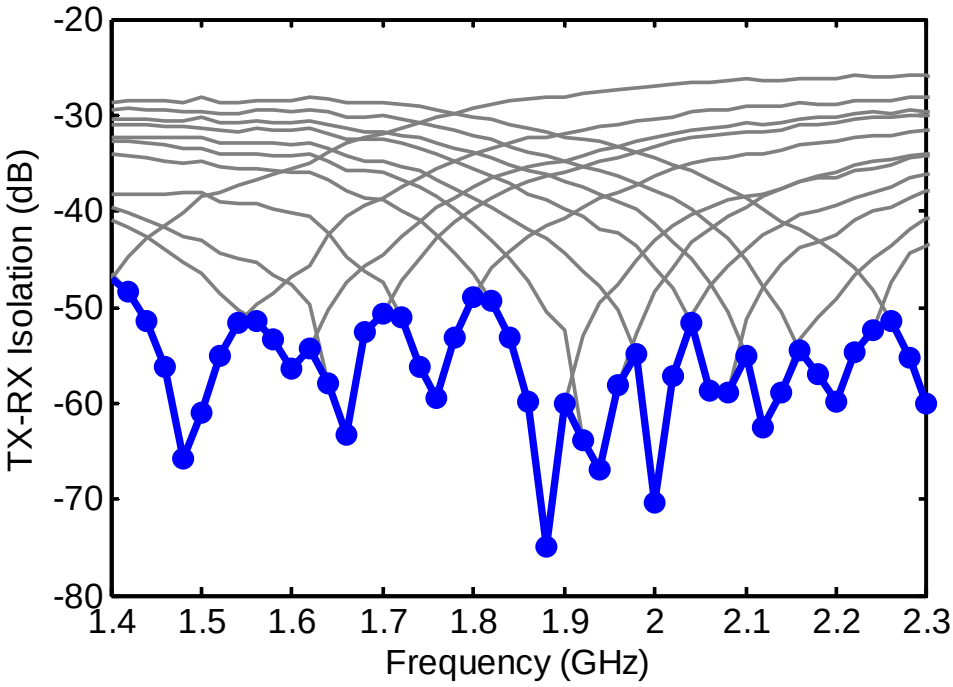


Figure 4.25: Measured TX-RX isolation for $R_{ANT} = 50\Omega$.

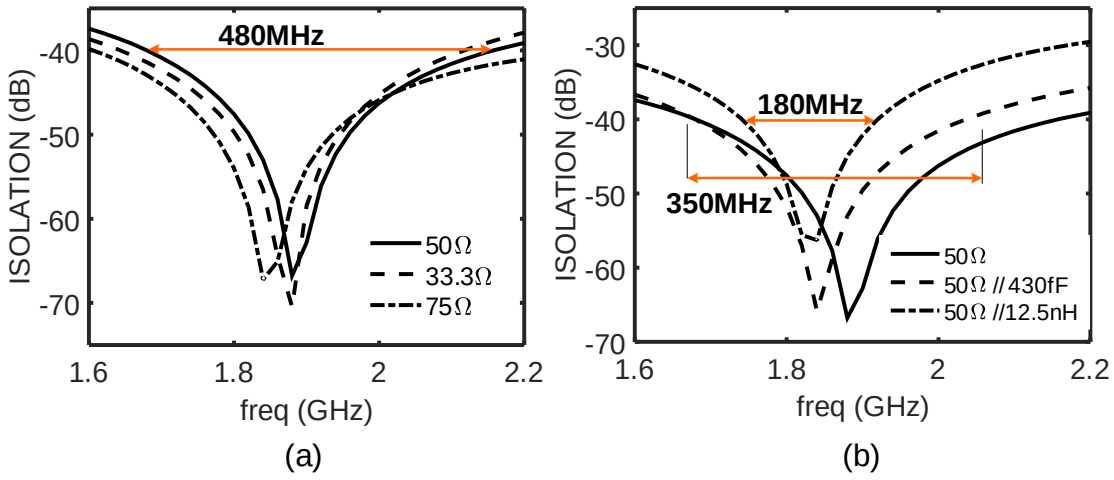


Figure 4.26: Simulated TX-RX isolation for different Z_{ANT} at , (a) different ANT resistances (VSWR $\sim$ 1.5), (b) different parallel ANT reactances (VSWR $\sim$ 1.3).

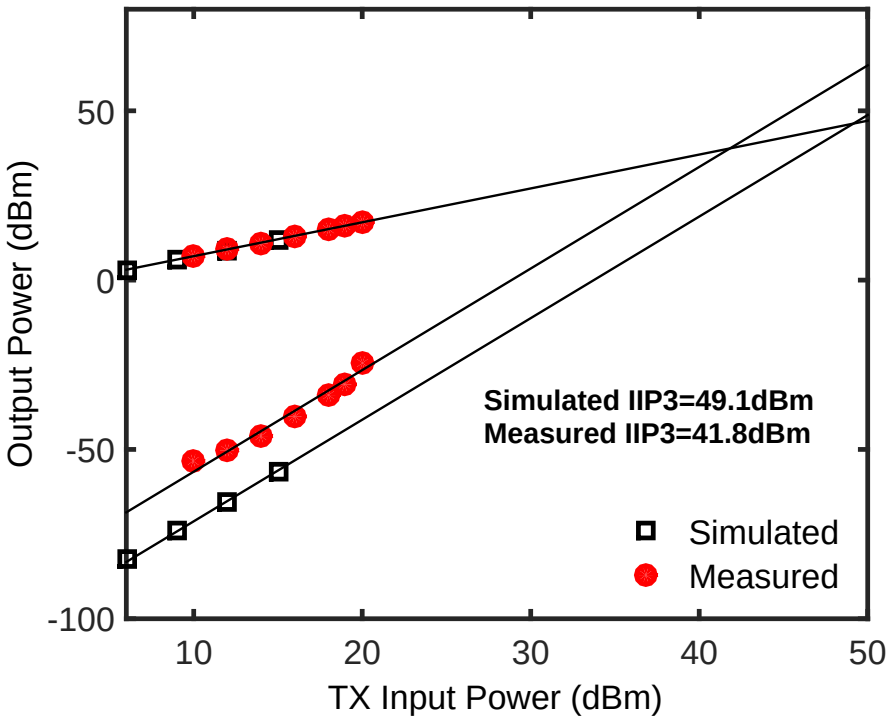


Figure 4.27: Simulated and measured $IIP3$ at TX input with two tones at 1.8725 GHz and 1.8775 GHz. The measured $IIP3$ is limited by PA $OIP3$ to around 41.8 dBm. By de-embedding the PA non-linearity, the measured $IIP3$ of the duplexer is about 45.7 dBm.

The high-power operation and linearity measurements of the duplexer are done using three test setups: i) two-tone test at the TX input, ii) a jammer at full-duplex separation from TX signal, iii) triple-beat (TB) test. For the two-tone test, a high power external PA (mini-circuits ZHL-16W-43X+) is used with an output-intercept point ($OIP3$) of 44.1 dBm at the PA pin of the duplexer (including the losses of the isolator, cables and traces). Fig. 4.27 shows the simulated and measured input third order intercept-points ($IIP3$) of the duplexer at PA input. The frequencies of the measured two tones are adjusted at 1.8725 GHz and 1.8775 GHz while the input power is reported at the PA input pin of the chip. Furthermore, a 30 dB attenuator

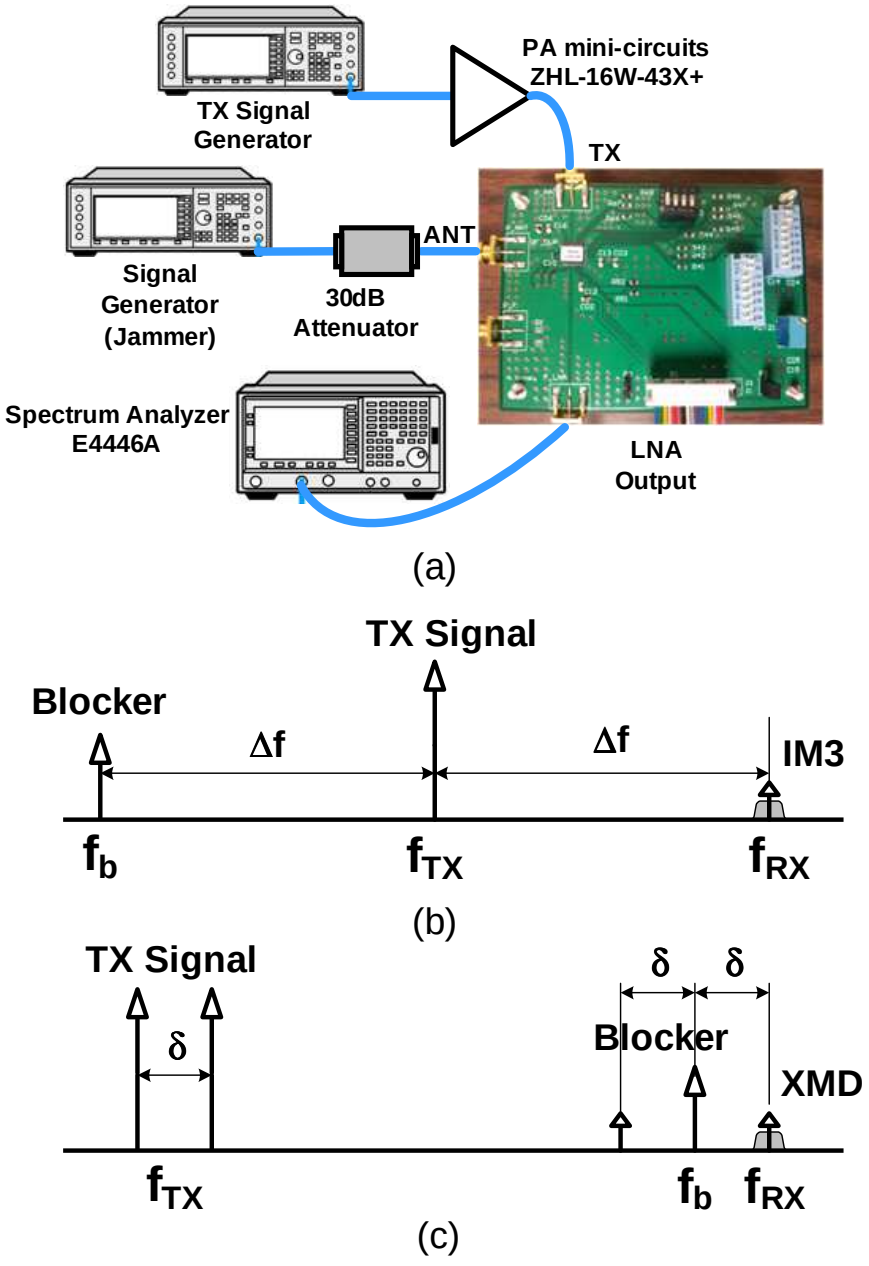


Figure 4.28: Conceptual figure to illustrate the settings for (a) setup for linearity measurement (b) full duplex separation blocker test, (**c**) tripple beat test.

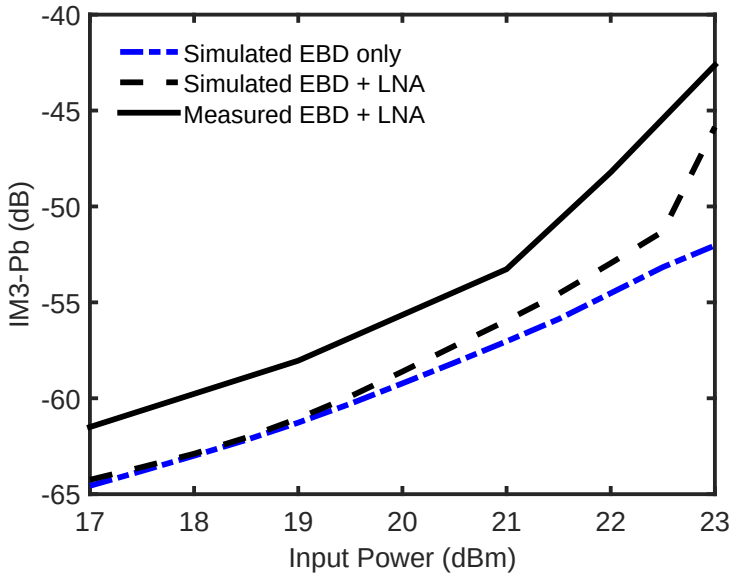


Figure 4.29: Simulated and measured $IM3$ resulting from the jammer at ANT port (f_{TX} =1.875GHz, f_{RX} =1.955GHz with 80MHz full duplex (FD) separation separation, P_b =-30dBm and f_b =1.795GHz).

is added at the ANT output to protect the spectrum analyzer from the high power TX signal. The simulated $IIP3$ of the duplexer is 49.1 dBm. The measured $IIP3$ accounts for the non-linearity of the PA and the duplexer, it is limited by the $OIP3$ of the PA to around 41.8 dBm. The effect of the PA non-linearity can be de-embedded to calculate the measured $IIP3$ of the duplexer to be about 45.7 dBm.

The setup of the linearity measurement is shown in Fig. 4.28(a), where the TX signal along with a jammer (blocker at frequency f_b) at the ANT can cause a third order intermodulation ($IM3$) at the desired RX frequency. An attenuator is used to protect the signal generator from the high TX power at ANT port. A blocker at full-duplex (FD) separation from TX frequency is located at $f_b = f_{TX} - \Delta f$, where $\Delta f = f_{RX} - f_{TX}$, as shown in Fig. 4.28(b). Fig. 4.29 shows the results assuming Δf =80 MHz (frequency separation in UMTS Band II), f_{TX} =1.875 GHz,

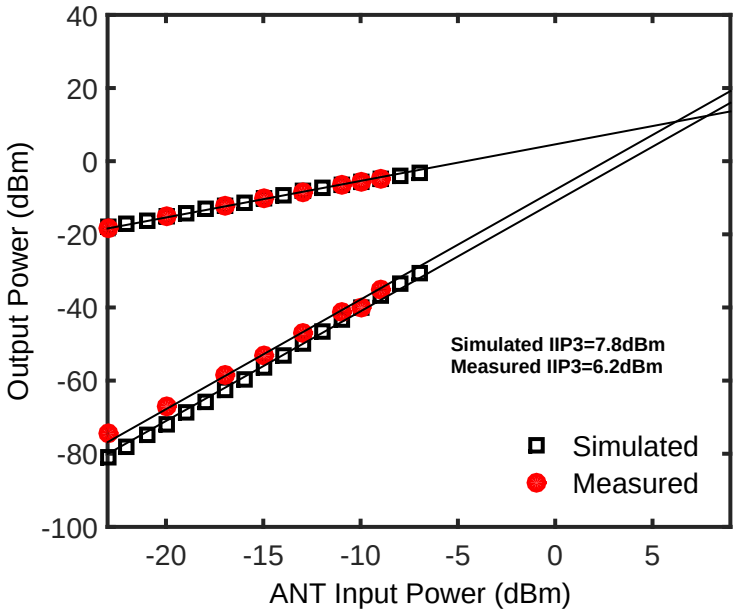


Figure 4.30: Simulated and measured receiver $IIP3$ with two tones 1.95 GHz and 1.96 GHz at the ANT port.

and f_{RX} =1.955 GHz. The blocker power (P_b) was -30 dBm at 1.795 GHz at the ANT port. The $IM3$ at LNA output changes with slope +2 with P_{TX}. As shown in Fig. 4.29, the simulated $IM3$ level for EBD without LNA is very close to that of EBD with LNA, which indicates the non-linearity is dominated by the EBD up to 20 dBm TX power. The measured results show that the duplexer has about -50 dB $IM3$ to P_b at P_{TX} = 22 dBm (P_{ANT} =18.8 dBm). P_b =-30 dBm was used instead of P_b =-15 dBm for 3GPP standard, since very high blocker power modulates the floating Z_{BAL}causing unacceptable $IM3$.

The triple-beat test of the duplexer was measured to determine the output cross-modulation distortion (XMD) up to P_b =-30 dBm at $f_b = f_{RX} - \delta$ (δ =5 MHz) [92], as shown in Fig. 4.28(c). For TX signal containing two sinusoidal tones with total power of 22 dBm (P_{ANT} =18.8 dBm) and 5 MHz separation, XMD to P_b ratio

equals -53.5 dB, or input referred XMD at ANT = −96.5 dBm for P_b =-43 dBm (3GPP standard). The proposed EBD linearity is still not sufficient to replace SAW duplexers, since the main objective of the prototype was to prove that the proposed cross-connected transformers structure can be used as an EBD with high TX-RX isolation. The receiver linearity is also measured using the two-tone test at the ANT port, which is highly affected by the linearity of the LNA since signals propagate from ANT to LNA directly. Fig. 4.30 shows that the $IIP3$ at the RX side is close to 6.2 dBm. This high linearity is achieved by using NMOS-PMOS inverter based transconductance LNA with adjusted biasing to achieve high linearity. The high overdrive voltages of NMOS (∼150 mV) and PMOS (∼320 mV) support achieving high linearity in converting the input voltage to current while the voltage swing at LNA output is maximized by centering the dc of the drain of NMOS/PMOS near half the supply voltage. For out-of-band $IIP3$, where two-tone test at 1.795 GHz and 1.875 GHz generates $IM3$ product at 1.955 GHz, the measured $IIP3$ is 5.9 dBm.

The chip performance is summarized in Table 4.2 with a detailed comparison with state-of-the-art integrated duplexers and a commercially available off-chip SAW duplexer. The hybrid transformer duplexer in [82] achieves excellent $TXIL$ and cascaded NF, but it cannot handle high power since it has no common-mode isolation. A differential version of the duplexer is used in [83] and [91] to enable high-power operation by improving the common-mode isolation at the expense of higher insertion loss. In [86], a step-down transformer is used in a dual-notch balancing network to enhance power handling and linearity, but it suffers from a large $RXIL$. Recently, a hybrid transformer EBD with single-ended LNA is reported [87], where a shunt capacitor is added to Z_{BAL} at the BAL port to compensate for the capacitive coupling. However, since the compensation path is indirect, it has a different transfer function through the hybrid transformer than the direct capacitive coupling reducing TX-RX

isolation bandwidth. The excellent linearity performance of [87] is attributed to two main factors. First, it has a technology advantage by using a partially depleted SOI process, which has smaller junction parasitics compared to bulk. The process also has a high substrate resistance and three very thick metals that minimize insertion losses. Second, it uses two extra inductors in Z_{BAL} network to create a two-notch isolation profile that relaxes the impact of parasitics on bandwidth of TX-RX isolation. This considerably increases the area of the duplexer ($\sim$5x compared to this work).

The proposed duplexer is implemented using a standard 0.18μm CMOS process with a single thick metal layer and achieves excellent $TXIL$, while supporting up to 22 dBm TX input power. The proposed EBD has a minimum effect of capacitive coupling on the bandwidth of TX-RX isolation. Furthermore, it can be used for medium power applications where the area is critical since it occupies small active area ($\sim$0.35 mm^2). The linearity performance is limited compared to [83, 87, 91], because of the complexity of the tunable floating balancing network. The EBD NF and linearity can be significantly improved by using an SOI technology and adding a wideband transformer to implement a differential Z_{BAL}. It employs a wideband transformer in Z_{BAL} to enhance cascaded NF by 1 dB and linearity performance of the duplexer by about 20 dB.

4.6 Conclusion

A widely-tuned fully-integrated FDD duplexer to support multi-band 3G/4G radios is highly desirable, to minimize the increasing cost and area of SAW/BAW duplexers. Integrated electrical balance duplexers (EBDs) are very promising to achieve high isolation between TX and RX bands with the advantage of tuning over a wide frequency range. However, designing a widely-tuned integrated duplexer with

Table 4.2: Performance Summary and Comparison with State-of-The-Art EBDs

	Murata SAYRF1G95C	Mikhemar [82] JSSC'13	Abdelhalem [83] MTT'13	Abdelhalem [91] MTT'14	Van Liempd [86] ESSCIRC'14	Van Liempd [87] ISSCC'15	This Work
Technology	SAW	65nm CMOS	90nm CMOS	90nm CMOS	0.18μm CMOS	0.18μm SOI	0.18μm CMOS
frequency Range	1 band	1.5-2.1 GHz	1.7-2.2 GHz	1.7-2.2 GHz	1.78-2 GHz	1.9-2.2 GHz	1.6-2.2 GHz
Z_{BAL} Tuning	N/A	2 dims.	2 dims.	4 dims.	4 dims.	4 dims.	2 dims.
ISO. TX Band	57 dB	$>$ 50 dB	$>$ 50 dB	$>$ 50 dB	$>$ 50 dB	$>$ 50 dB	$>$ 50 dB
ISO. RX Band	50 dB	45 dB	40 dB	50 dB	40 dB††	45 dB	40 dB
Z_{ANT} Impedance	N/A	50Ω	50Ω	2:1 VSWR	SkyCross ant.	1.5:1 VSWR	1.3:1 VSWR
Common-mode ISO.	N/A	0 dB	$>$ 60 dB	$>$ 60 dB	poor	single-ended	single-ended
$TXIL$	2.7 dB*	2.5 dB	4.7 dB†	4.5 dB†	3.0 dB	3.7 dB	3.2 dB
Cas. RX NF	5.5 dB**	5 dB	6.7 dB†	6.7 dB†	11 dB (w/o LNA)	3.9 dB (w/o LNA)	6.5 dB
Max. P_{TX}	$>$ 30 dBm	$<$ 12 dBm	27 dBm	27 dBm	27 dBm	$>$ 27 dBm	22 dBm
TX-to-ANT $IIP3$	N/A	N/A	N/A	N/A	48 dBm	70 dBm	45.7 dBm
Sim. Z_{BAL} $IIP3$	N/A	N/A	N/A	54 dBm	N/A	65 dBm	43.5 dBm
RX-to-ANT $IIP3$	N/A	N/A	-5.6 dBm	-4.6 dBm	32 dBm (w/o LNA)	72 dBm (w/o LNA)	6.2 dBm
Area [mm^2]	3.2	0.1 incl. LNA	0.6 incl. LNA	2.2 incl. RX	0.67	1.75	0.35 incl. LNA

*Including 1.1dB loss, assuming Skyworks AS195-306 SP5T switch and 0.3dB PCB Loss,
**Including 2dB for typical LNA NF plus 1.1dB loss (for switch and PCB),
†Including 0.8dB loss, assuming Anaren BD1722N5050AHF antenna balun, ††With real Z_{ANT}.

competitive insertion loss and linearity performance is very challenging. A wideband tunable EBD with a single-ended LNA is proposed by employing a floating balancing impedance. It enables RF power operation up to 22 dBm while achieving higher than 50 dB TX-RX isolation from 1.6-2.2 GHz. A comprehensive analysis for different configurations of passive EBDs is presented, showing the sources of losses of the duplexer and their effect on noise figure and insertion loss. This work presents a step forward to replace today's band-specific SAW/BAW duplexers with a fully integrated low-loss wideband duplexer.

5. ANALYSIS OF INTEGRATED ACTIVE ELECTRICAL BALANCE DUPLEXERS

5.1 Introduction

The concept of active EBD is also introduced and analyzed in this chapter to achieve lower $TXIL$ and NF. Active TX suppression techniques were reported previously to provide additional isolation for a low performance passive duplexer by TX replica cancellation [69, 93, 94] and by TX filtering using M-phase passive-mixer-based high-Q band pass filters [72, 73]. However, these techniques still rely on passive duplexers and are not suitable for high power applications. A direct active EBD was reported only in [95] to enhance the total power efficiency of the duplexer using a rectifier to convert the RF power consumed in the lossy EBD to dc. In this chapter, an active EBD is proposed to achieve better insertion loss than the theoretical limit of passive EBDs. The concept of TX current cancellation is analyzed and compared to [95] in terms of noise figure and power efficiency.

5.2 Active Integrated EBDs Theory

All duplexers in the previous section were passive and required an extra balancing impedance to achieve the desired isolation. Since active devices are non-reciprocal, they can provide an advantage to passives in terms of insertion loss ($TXIL$ and $RXIL$). However, these devices consume more dc power and this dc power consumption should be included in the power transfer efficiency of the duplexer. The proposed figure of merit (FOM_2) of the active EBDs, considering dc power consumption effect, is formulated as:

$$FOM_2 = NF + 10\ \log_{10}\left(\frac{\eta_{PA}\left(P_{DC} + P_{ACTIVE}\right)}{P_{ANT}}\right) \tag{5.1}$$

where η_{PA} is the efficiency of the PA at the transmitter, P_{DC} is the dc power consumed by the PA and P_{ACTIVE} is the dc power consumed by the active circuit of the duplexer. Active EBDs can be categorized based on two major techniques. The first technique is the TX power reuse proposed in [78] by converting the TX power consumed in R_{BAL} to dc power. The second technique proposed in this thesis employs TX current cancellation. P_{ACTIVE} is different depending on the type of the active EBD; it is negative for power reuse EBDs, while it is positive for TX current cancellation EBDs. The main parameters that define the performance of active EBDs are power efficiency, noise figure, and linearity. FOM_2 can be used to compare active EBDs with the same linearity, since there is a trade-off between power efficiency and linearity.

5.2.1 TX RF Power Reuse EBDs

The idea of the power reuse is to use an RF-dc converter instead of the balancing resistance. A rectifier is used to convert the RF power to dc current input to the battery. The EBD, in [95], used this technique as shown in Fig. 5.1. A class E RF-dc converter is used for its high efficiency. To preserve the functionality of the duplexer, the effective impedance seen at the input of the rectifier should be matched to the antenna impedance, however due to the rectifier nature the input impedance is varying with the input power. Thus the linearity of this duplexer is not acceptable except if the TX power has certain defined power level range. Another problem in the power reuse technique is its power efficiency. If the rectifier can convert the power at BAL port to dc by efficiency η_{BAL}, then $P_{ACTIVE} = -\eta_{BAL}P_{BAL}$. If the transformer loss is ignored, the FOM_2 in (5.1) can be expressed as:

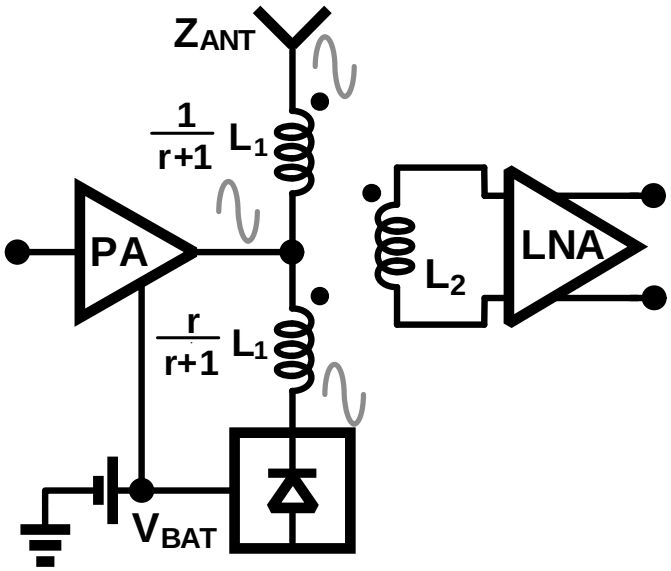


Figure 5.1: Power reuse active EBD circuit [95].

$$FOM_2 = 10\,\log_{10}(1+r) + 10\,\log_{10}\left(\frac{1+r}{r} - \frac{\eta_{PA}\,\eta_{BAL}}{r}\right) \tag{5.2}$$

Assuming $\eta_{BAL} = 60\%$ reported in [95], and $\eta_{BAL} = 50\%$ which represents a highly efficient linear PA at $r = 1$, FOM_2 is enhanced from 6dB to 5.3dB. Since FOM_2 is varying with r, there is a value for r to provide minimum FOM_2 $r_{opt1} = \sqrt{1 - \eta_{PA}\,\eta_{BAL}}$, and $FOM_{2,min}$ is calculated by:

$$FOM_2 = 10\,\log_{10}(1+r) + 10\,\log_{10}\left(\frac{1+r}{r} - \frac{\eta_{PA}\,\eta_{BAL}}{r}\right) \tag{5.3}$$

From the analysis, r_{opt1} is slightly less than 1 depending on the values of η_{BAL} and η_{PA}. The power efficiency of this technique is even worse for lower η_{PA} which makes this technique difficult to use in practice.

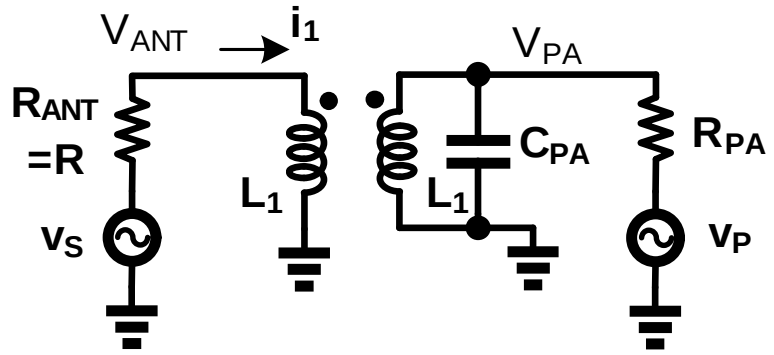


Figure 5.2: A transformer coupling between ANT and TX ports.

5.2.2 TX Current Cancellation EBDs

On analyzing a simple circuit with two ports ANT and PA, and an ideal transformer as shown in Fig. 5.2, a TX signal modeled by voltage source v_P can be canceled with a concept similar to noise cancellation reported in [96]. Current drawn from ANT port $i_1 = (v_S - v_P) / (R + R_{PA})$, where v_S is a voltage source modeling the RX signal and R_{PA} is the source resistance of the PA. i_1 can be used with another voltage signal to cancel v_P. The voltage at the ANT port V_{ANT}, it contains a component of v_P, but with same sign as v_S. V_{ANT} is calculated by:

$$V_{ANT} = v_S - i_1 R = \frac{v_S R_{PA} + v_P R}{R + R_{PA}}. \tag{5.4}$$

To cancel the TX signal (v_P), i_1 and V_{ANT} must be added together with correct weights as defined by V_{RX2}:

$$V_{RX2} = V_{ANT} + i_1 R. \tag{5.5}$$

The main difficulty of the TX cancellation is how to add these two signals together. This addition can be in terms of voltages or currents. For a voltage addition,

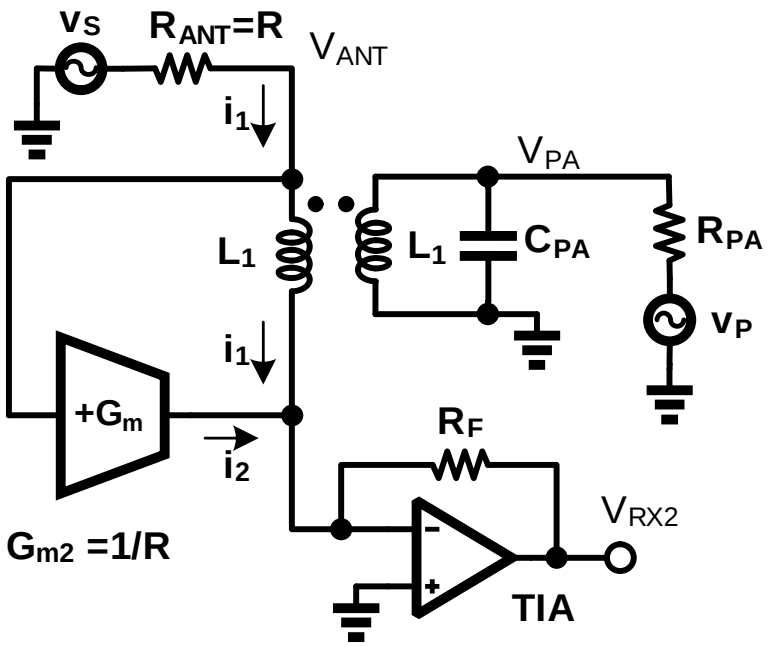


Figure 5.3: Proposed concept of active EBD using TX current cancellation.

i_1 is converted to a voltage by a resistance, which results in an increased higher effective $TXIL$. Furthermore, this resistance will add an extra noise source. This voltage addition operation is similar to the voltage-mode passive EBD (configuration 2). On the other hand, for a current addition, a transconductance (G_{m2}) is needed to convert V_{ANT} to current, where its output current is added to i_1 to cancel TX signal as shown in Fig. 5.3. The advantage of this method is its high power efficiency since the TX voltage at the output of the transconductance is zero or the transconductance does not provide any real output power. A trans-impedance amplifier (TIA) is used to convert the current to output voltage with very low input impedance. The output voltage V_{RX2} is calculated by:

$$V_{RX2} = R_F \left(G_{m2} V_{ANT} + i_1 \right) = v_S \frac{R_F}{R}, \tag{5.6}$$

where R_F is the feedback resistance of the TIA. Another advantage of this method is the diminished effect of the TIA noise since RF can be very large relative to R. Furthermore, using an ideal transformer, the $TXIL$ is zero, since the TX voltage of the PA is completely applied on the antenna. This means that the duplexer FOM_2 is enhanced by 3dB ignoring the power consumed in G_{m2}.

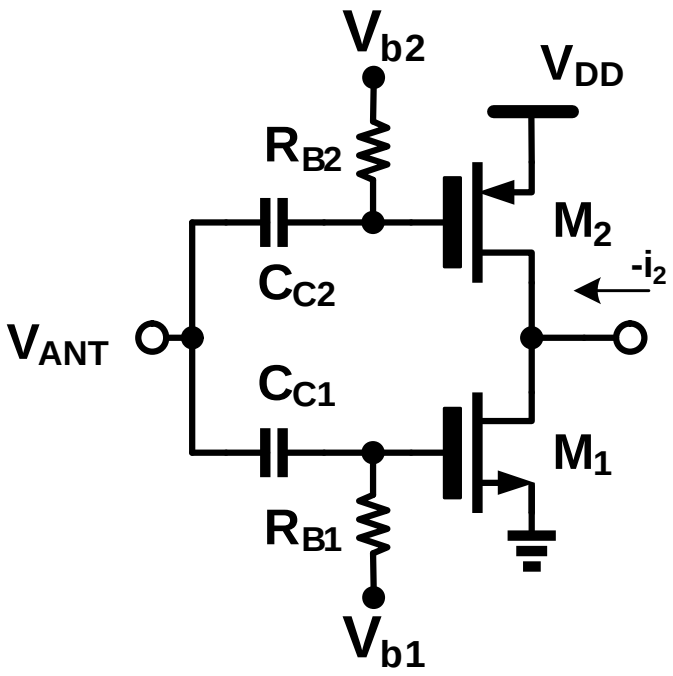


Figure 5.4: Proposed concept of active EBD using TX current cancellation.

To be able to handle large input TX voltage, the transconductance G_{m2} should have linear output current with the high input voltage. The proposed transconductance, shown in Fig. 5.4, is similar to the class AB power amplifier in [97], where NMOS and PMOS transistors are used to achieve very high linear transconductance. Thick gate high voltage devices are used to support higher gate voltage. Transistors M_1 and M_2 are biased such that at zero input they are in the saturation region. For

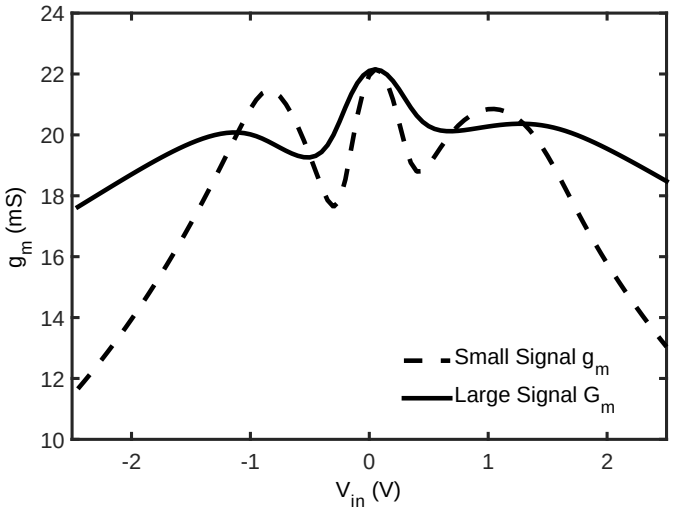


Figure 5.5: Simulated transconductance variation with input voltage v_{in}.

a large positive (negative) voltage, M_1 (M_2) is working in velocity saturation and M_2 (M_1) is off.

The advantage of velocity saturation region is having constant G_{m2} with input voltage. The dc current consumed can be approximated by $I_{dc} = I_{peak}/\pi = (G_{m2}\, V_{peak})/\pi$, where I_{peak} is the peak of the RF output current and V_{peak} is the peak of RF input voltage. The maximum applied V_{peak} ($V_{p,max}$) on the transconductance is defined by $V_{p,max} = V_{BD} - V_{b1}$, where V_{BD} is the breakdown gate-source voltage of the MOSFET device, and V_{b1} is the biasing gate-source voltage. The transconductance variation with input voltage is shown in Fig. 5.5. The small signal g_m is defined by the first derivative of output current (I_{out}) with V_{in}, while the large signal is defined as I_{out}/V_{in}. Using 0.18μm CMOS process, and thick voltage 3.3V devices for high breakdown voltage, the variation of the large signal G_{m2} is smaller than $\pm$10% for input range up to $\pm$2.5 V. In practice, the large signal G_{m2} is required to track the variation of Z_{ANT} in order to cancel TX signal efficiently. Furthermore,

G_{m2} is adjusted to have optimum TX cancellation at the maximum operating TX voltage, while at lower TX voltage the slight degradation in isolation is tolerable. The maximum applied voltage on the G_{m2} is related to the breakdown voltage of the transistors. The total power consumed by G_{m2} (P_{ACTIVE}) can be calculated by:

$$P_{ACTIVE} \approx \frac{V_{DD}\, V_{peak}}{\pi\, R} \approx \frac{2\, V_{DD}}{\pi\, V_{peak}}\, P_{ANT}. \tag{5.7}$$

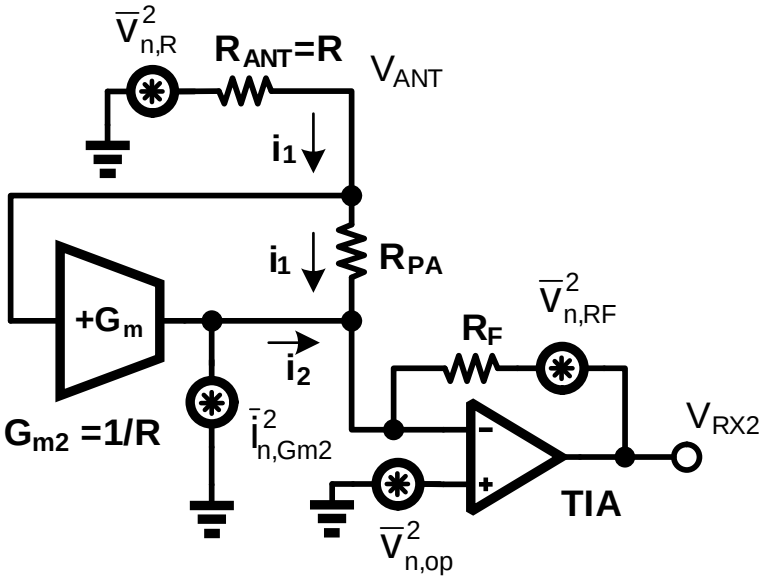


Figure 5.6: Active EBD with noise sources to calculate NF.

The noise figure of the receiver can be found using the noise model illustrated in Fig. 5.6. Assuming a high gain opamp in the TIA, the input impedance of the TIA is very low at the required frequency range. The total output noise at V_{RX2} is calculated by:

$$\overline{v}^2_{n,o} = \overline{v}^2_{n,R}\, \frac{R_F^2}{R^2} + \bar{i}^2_{n,Gm2}\, R_F^2 + \left(1 + \frac{R_F}{R + R_{PA}}\right)^2 \overline{v}^2_{n,op} + \overline{v}^2_{n,RF}. \tag{5.8}$$

where $\overline{v}_{n,R}^2$ is the noise due R_{ANT}, $\overline{i}_{n,Gm2}^2$ is the noise due to G_{m2}, $\overline{v}_{n,op}^2$ is the noise due to TIA s' opamp and $\overline{v}_{n,RF}^2$ is the noise due to R_F. The noise figure is calculated by:

$$NF = 10\,\log_{10}\left(1+\gamma+\left(\frac{R}{R_F}+\frac{R}{R+R_{PA}}\right)^2\frac{\overline{v}_{n,op}^2}{\overline{v}_{n,R}^2}+\frac{R}{R_F}\right). \tag{5.9}$$

If $R_F \gg R$ and $\overline{v}_{n,op}^2 \ll \overline{v}_{n,op}^2$, NF can be simplified to $10\,\log_{10}(1+\gamma)$. Using $P_{TX} = \eta_{PA}\,P_{DC} = P_{ANT}$, the FOM_2 of the active EBD can be calculated from (5.1) and (5.7) by:

$$FOM_2 = 10\,\log_{10}(1+\gamma) + 10\,\log_{10}\left(1+\frac{2\eta_{PA}\,P_{DC}}{\pi\,V_{Peak}}\right). \tag{5.10}$$

Assuming $\gamma = 1$, $V_{DD} = 1.8\,\mathrm{V}$, $V_{peak} = 1\,\mathrm{V}$ ($P_{ANT} = 10$ dBm), and $\eta_{PA} = 40\%$, $FOM_2 = 4.64$ dB which is less than the theoretical limit of passive EBDs ($\sim$ 6dB) without considering the effect of transformer loss.

5.3 Active Integrated EBDs Implementation

Two different implementations of TX current cancellation EBD were designed and simulated using 0.18μm CMOS process for 1.7-2.1 GHz frequency band using TX current cancellation techniques as shown in Fig. 5.7(a) and (b). In Fig. 5.7(a), the transformer coupling loss will mainly affect $TXIL$, while NF will be close to ideal transformer case. v_{PA} was used for feed-forward cancellation, because the transconductance needs opposite signs for cancellation of TX signal and to avoid the effect of the transconductance input capacitance on ANT port impedance. C_{BAL} is used to adjust the phase of i_2 to cancel i_1 at the required frequency. Furthermore, an extra tunable capacitance at ANT port can be used to support inductive ANT impedance. C_{BAL} and G_{m2} should be tunable to track the variation of the ANT impedance versus frequency. G_{m2} tunability is implemented by segmentation of

G_{m2} into segments, where each segment has NMOS and PMOS devices and can be activated or deactivated using a digital switch.

In the second prototype shown in Fig. 5.7(b), transformer loss affects mainly the NF accompanied with a slight effect on $TXIL$ since i_1' is less than i_1 due to transformer coupling loss. C_{C3} is used to short the other terminal of L_2 at high frequencies, while preserving the dc voltage at the output node of G_{m2}. The polarity of the current is adjusted by using a transformer with negative k. Fig. 5.8(a) and (b) show the simulated variation of large signal NF and effective $TXIL$ with the output TX power at the antenna ($P_{ANT,TX}$) in case of $f_{RX} = f_{TX} + 80$ MHz. The increase of NF with input TX power (P_{TX}) is due to the switching action of M_1 and M_2 noise sources of G_{m2}, since flicker noise close to dc and thermal noise at harmonics of $2\,f_{TX}$ are converted to f_{TX}. For the effective $TXIL$ ($TXIL_{eff}$), η_{PA} variation with P_{TX} is modeled by $\eta_{PA} = \eta_{max}\sqrt{P_{TX}/P_{13dBm}}$, where P_{13dBm} (or 20 mW) is the rated power for the duplexer where $\eta_{max} = 50\,\%$.

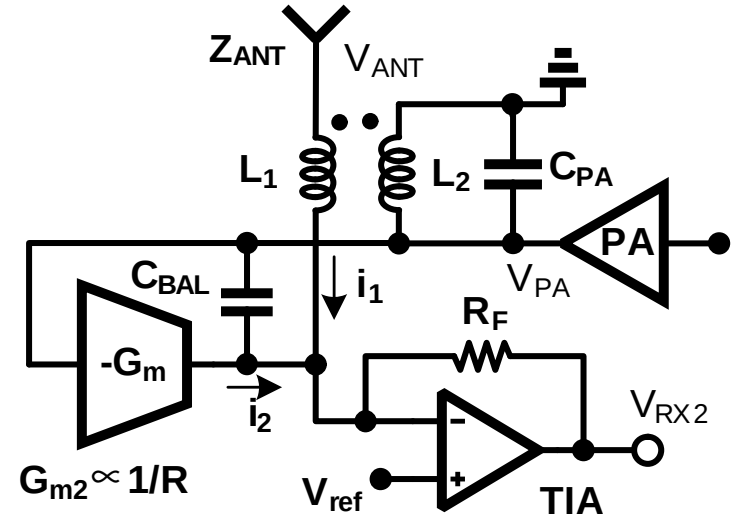
As seen in Fig. 5.8, FOM_2 is higher than theoretical analysis due to: the increase in NF by more than 1 dB at high $P_{ANT,TX}$ and due to the increase in $TXIL_{eff}$ at low $P_{ANT,TX}$. The minimum FOM_2 is at mid-range.

The linearity of the two active EBDs was tested by measuring the change of TX-RX isolation with P_{TX} as shown in Fig. 5.9(a) and (b). The TX isolation was adjusted for TX cancellation at $P_{TX} = 13$ dBm at$f_{TX} = 1.85$ GHz. The TX isolation is below -35 dB for $P_{TX} = 2$ dBm to 13 dBm. The harmonic distortion due to the TX signal is plotted as an indication of the linearity of G_{m2}. Harmonic distortion $HD2$ and $HD3$ are less than -35dB. Furthermore, the full duplex separation test is used to test the linearity of the duplexer, where a blocker at the ANT port (at $f_b = 2\,f_{TX} - f_{RX}$) is used to inter-modulate with TX signal. The third intermodulation ($IM3$) ratio to blocker power (P_b) variation with input TX power is shown in Fig.

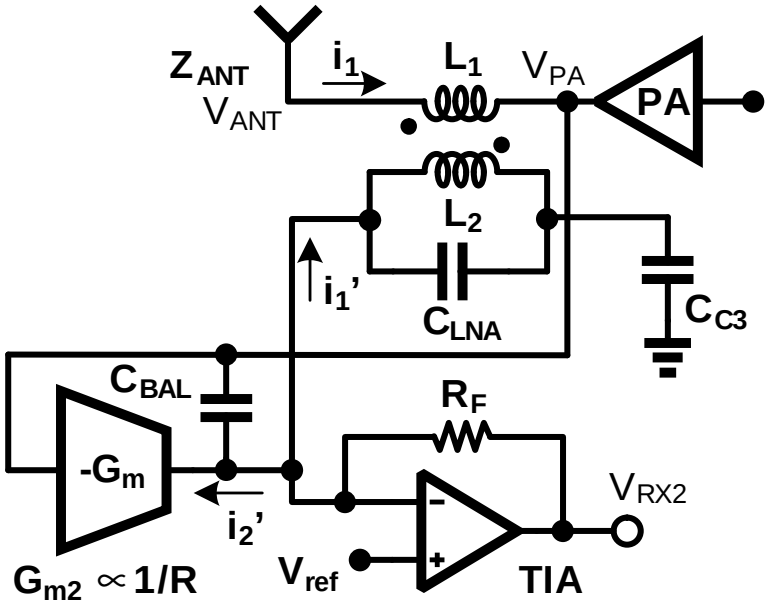
5.9, where $P_b = -30$ dBm and $f_b = f_{TX} - 80$ MHz. $IM3 - P_b$ ratio increases with P_{TX} till $P_{TX} = 0$ dBm then decreases having two minima and increases again. The reason for this behavior is the nature of G_{m2} demonstrated in Fig. 5.5, where the large signal G_{m2} is changing with P_{TX}. Furthermore, the worst $IM3 - P_b$ happens close to the local minima of the small signal G_{m2}. It is clear that the two major drawbacks of active EBDs are their linearity performance and the increase of NF with the input TX power. These drawbacks can be enhanced by improving the high power transconductance in the active EBD.

5.4 Conclusion

Active EBDs can have better insertion loss compared to passive EBDs at the cost of worse linearity and higher NF at higher TX power. Two practical designs of active EBDs, based on TX current cancellation, were proposed. They can operate up to 13 dBm TX output power at the antenna, and achieves 3dB better FOM compared to passive EBD. However, they suffer from linearity problems that limit the range of the input TX power and the maximum tolerable blocker power.



(a)



(b)

Figure 5.7: Real implementation of EBD using TX current cancellation (a) first prototype favoring NF, (b) second prototype favoring $TXIL$.

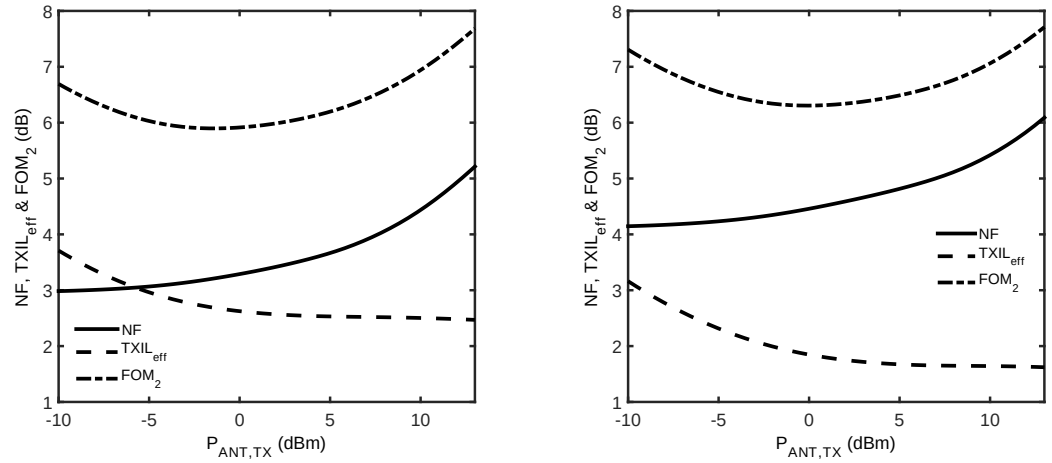


Figure 5.8: Simulated NF, effective $TXIL$ and FOM_2: (a) first prototype, (b) second prototype ($P_{ANT,TX} = P_{TX} - TXIL$)

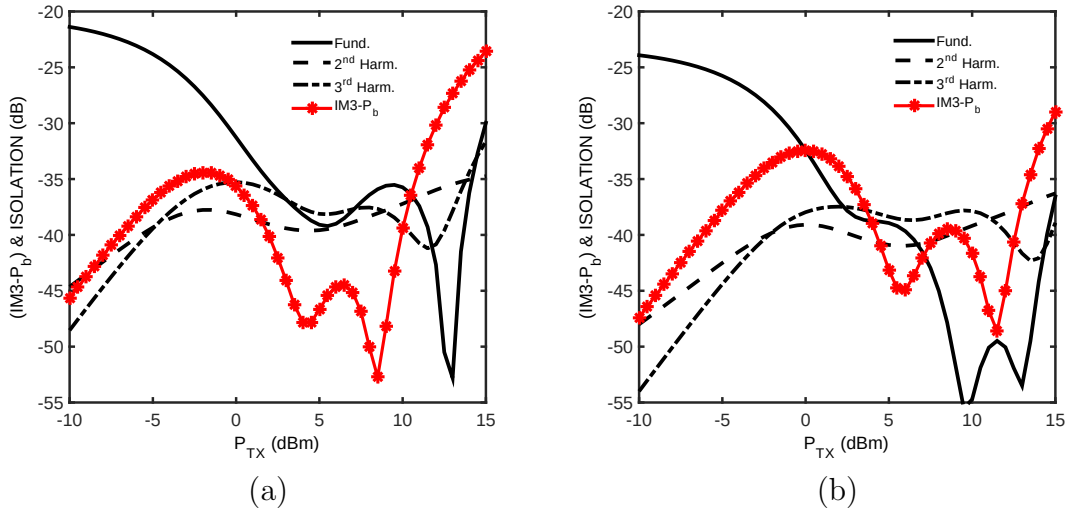


Figure 5.9: Simulated isolation change with P_{in} at f_{TX} fundamental, 2^{nd} harmonic and 3^{rd} harmonic for: (a) first prototype, (b) second prototype.

6. CONCLUSION AND FUTURE WORK

6.1 Conclusion

The dissertation focuses on the integration of radio frequency (RF) biochemical sensors and frequency division duplex (FDD) RF duplexers. The integration of RF biochemical sensors are explored by two proposals: 1) a high accuracy chemical sensor measuring real relative permittivity ε_r' at 10 GHz, 2) a wideband dielectric spectroscopy sensor system that can measure complex permittivity (ε_r' and ε_r'') in 1-6 GHz range.

The high accuracy chemical sensor, fabricated in IBM 90 nm CMOS technology, has a self-sustained fractional-N PLL-based CMOS sensing system to measure the dielectric constant of organic chemicals and their mixtures at precise microwave frequencies. System sensitivity is improved by employing a reference VCO, in addition to the sensing VCO, which tracks correlated low-frequency drifts. A simple single-step material application measurement procedure is enabled with a low-complexity bang–bang control loop that samples the difference between the control voltage with the sensor and reference oscillator in the PLL loop and then adjusts a fractional frequency divider. Binary mixture characterization of organic chemicals shows that the system was able to detect mixture permittivities with fractional volume down to 1%. Overall, the high-level of integration and compact size achieved in this work makes it suitable for lab-on-chip and point-of-care applications. The dc power consumption is less than 22 mW.

The spectroscopy system is proposed using LC-based oscillator capacitive sensing. The system is fabricated using IBM 0.18 μm CMOS technology and tested with less than 24 mW dc power consumption. The sensor can measure the complex

permittivity of different materials including de-ionized water and PBS at multiple frequencies in the 1-6 GHz range. The system has a reference oscillator to alleviate the effects of the temperature and drifts using a correlated double sampling (CDS) technique with 2.1 ppm random noise in frequency shift reading and 110 ppm in current shift reading. The sensor was tested with ethanol-water mixtures with different concentrations and achieved a maximum error of 2% in real permittivity and 5% in imaginary permittivity in 1-3.8 GHz frequency range.

Integration of FDD RF duplexers has an enormous impact to avoid the high cost and the huge size of surface-acoustic-wave (SAW) duplexers. Integrated electric balance duplexers (EBDs) are the best candidate for replacing SAW duplexers while achieving high isolation between TX and RX bands with the advantage of tuning over a wide frequency range. However, EBDs suffer from high transmitter insertion loss ($TXIL$) and high noise figure (NF). To enhance $TXIL$ and NF, two proposed EBDs were designed and analyzed. The first one is passive EBD with single-ended LNA to avoid high power common-mode TX signal at the input of the differential LNA in the previously published EBDs. This passive is implemented in IBM 0.18 μm CMOS technology and tested. The second one is an active EBD which was not fabricated.

The wide-band tunable EBD with a single-ended LNA is proposed by employing a floating balancing impedance. It enables RF power operation up to 22 dBm while achieving higher than 50 dB TX-RX isolation from 1.6-2.2 GHz. A comprehensive analysis for different configurations of passive EBDs is presented, showing the sources of losses of the duplexer and their effect on noise figure and insertion loss. This work offers a step forward to replace today's band-specific SAW/BAW duplexers with a fully integrated low-loss wideband duplexer.

The simulated active EBDs have better insertion loss compared to passive EBDs

at the cost of worse linearity and higher NF at higher TX power. Two practical designs of active EBDs, based on TX current cancellation, were proposed. They can operate up to 13 dBm TX output power at the antenna, and achieves 3 dB better FOM compared to passive EBD. However, they suffer from linearity problems that limit the range of the input TX power and the maximum tolerable blocker power.

6.2 Recommendations for Future Work

6.2.1 Wideband High Frequency Flow Cytometer

The fabricated wideband spectroscopy system suffers from some drawbacks due to the technology used for fabrication. For more advanced technology with smaller feature size, the frequency gaps in the design can be avoided and the overlap between the frequency ranges is maximized. Furthermore, the frequency can be extended to higher frequencies. A flow Cytometer working between 1 GHz and 10 GHz can be used to differentiate between cells that have variation in their nuclei electric properties. The detection of this variations requires a very high sensitivity of the sensing electronic circuit and a stable microfluidic channel on the integrated circuit. Another drawback in the fabricated prototype is the low speed serial interface. Using faster interface will promote the speed of the reading of the differential admittance of the capacitive sensor till 100 kHz readout frequency to be suitable for flow Cytometer.

6.2.2 Fabrication of the Active Electrical Balance Duplexers

The active electrical balance duplexers (EBDs) in section 5.3 needs to be fabricated and measured. The purpose of these EBDs is to be used in systems which have SAW duplexers but didn't required high TX power. Another direction of the research in this area is to use reciprocal passive mixers [98] to filter the RX signal and TX signal from each other. As shown in Fig. 5.9, current $i_1 = V_{ANT}/R_{ANT}$ is summed to current $i_2 = j\omega C_{PA} V_{PA}$ after the passive mixers at the input of the TIA. i_1 and i_2

should be summed in a way to cancel TX signal and amplify RX signal. C_{PA} value will adjust the magnitude of TX signal of i_2 to match i_1, while θ is used to adjust the phase. Capacitor C_{PA} is used to convert V_{PA} voltage to current instead of resistance to avoid power consumption since capacitors are ideally are lossless elements. Since the receiver is designed to cancel TX signal, it also cancels the reciprocal noise due to phase noise of the clock f_{RX}. The implementation of this duplexer requires advanced node technology to support the passive mixer that support high TX current through its switches.

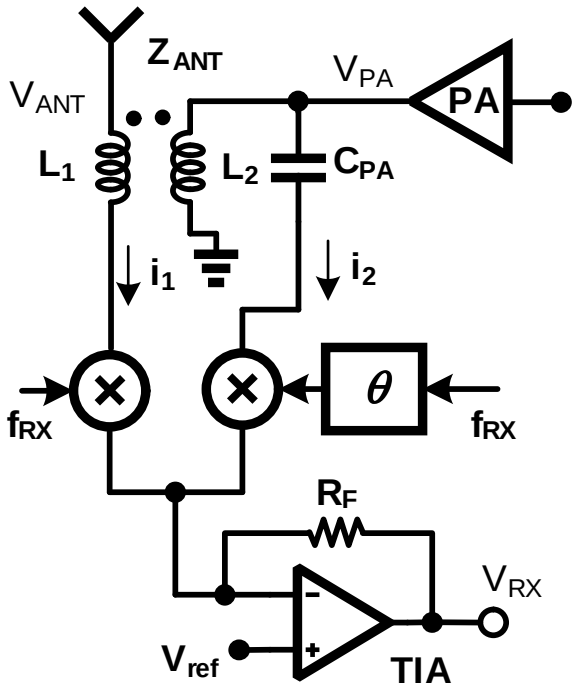


Figure 6.1: A TX cancellation active EBD using reciprocal passive mixing to achieve higher linearity and lower NF.

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